

URP5B98 mmWave PA



UltrabandTech

Product Overview

The URP5B98 is an P_{sat} of 25 dBm MMIC integrated the mmWave PA in die form, which is designed by using 0.15 μm GaAs pHEMT devices in a compact die size with excellent performance.

Key Features

- 24 – 30 GHz frequency range
- P_{sat} : 25 dBm
- PAE : 47%
- OIP3 : 32 dBm
- Die size : 1970 μm \times 970 μm

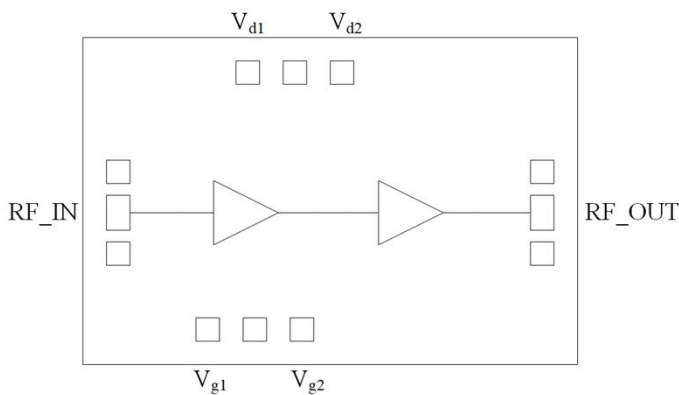
Application

- 5G FR2 Antenna Modules
- FWA
- Satcom
- Radar

Ordering Information

Part Number	Package
URP5B98	Die

Functional Block Diagram



Absolute Maximum Ratings

Parameters	Rating	Unit
DC Drain Voltage	10	V
CW Incident Power	>10	dBm
Operating temperature	-40°C to +85°C	°C
Storage Temperature	-65°C to +150°C	°C

Recommended Operating Conditions

Parameter	Value	Unit
V_{d1}, V_{d2}	5	V
V_{g1}	-0.45	V
I_{d1} (Quiescent)	44	mA
V_{g2}	-0.45	V
I_{d2} (Quiescent)	88	mA



Electrical Specifications ($T_A = 25\text{ }^\circ\text{C}$, $V_{d1}, V_{d2} = 5\text{ V}$, $V_{g1} = -0.45\text{ V}$, $V_{g2} = -0.45\text{ V}$, $Z_0 = 50\text{ }\Omega$)

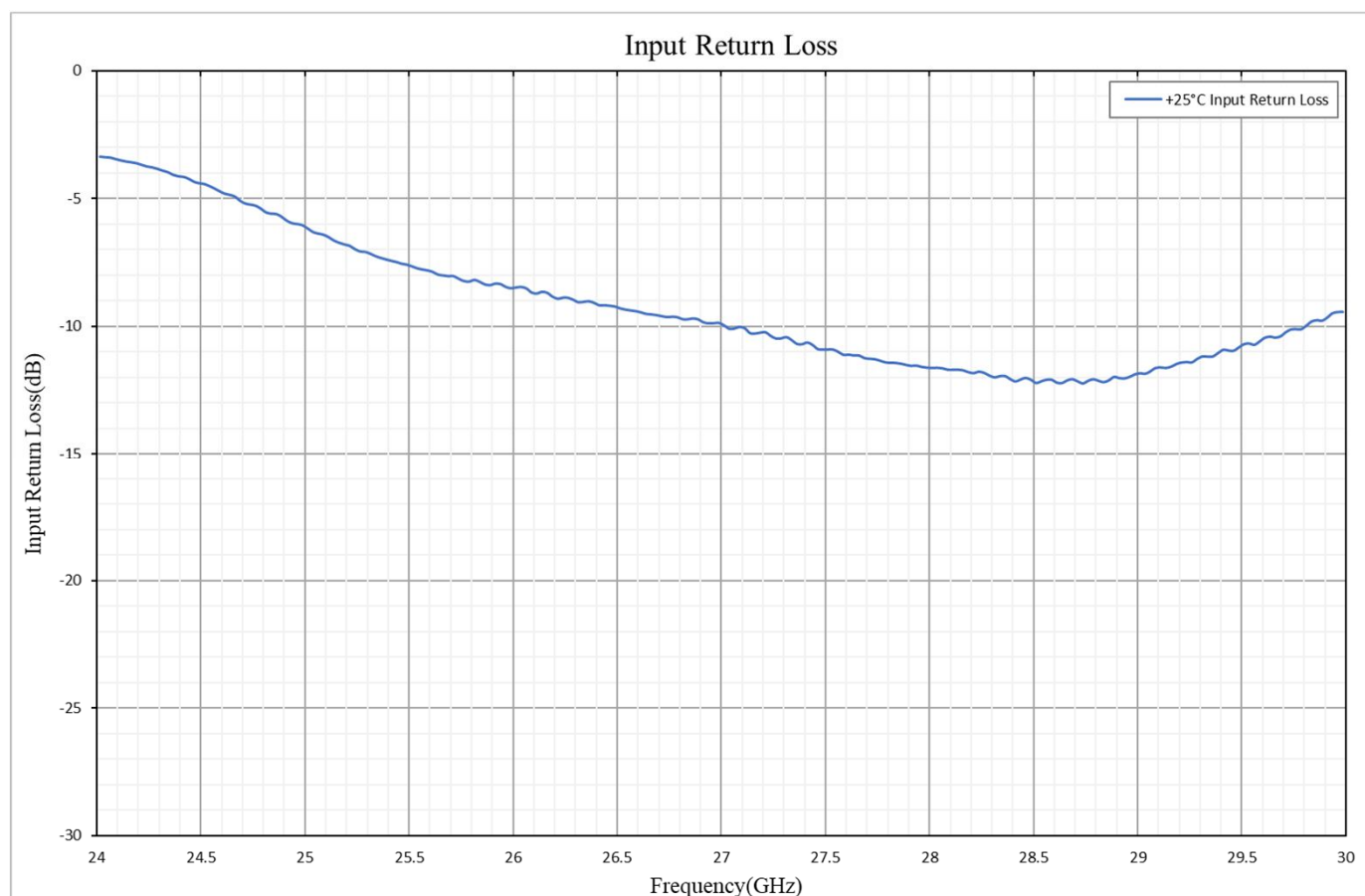
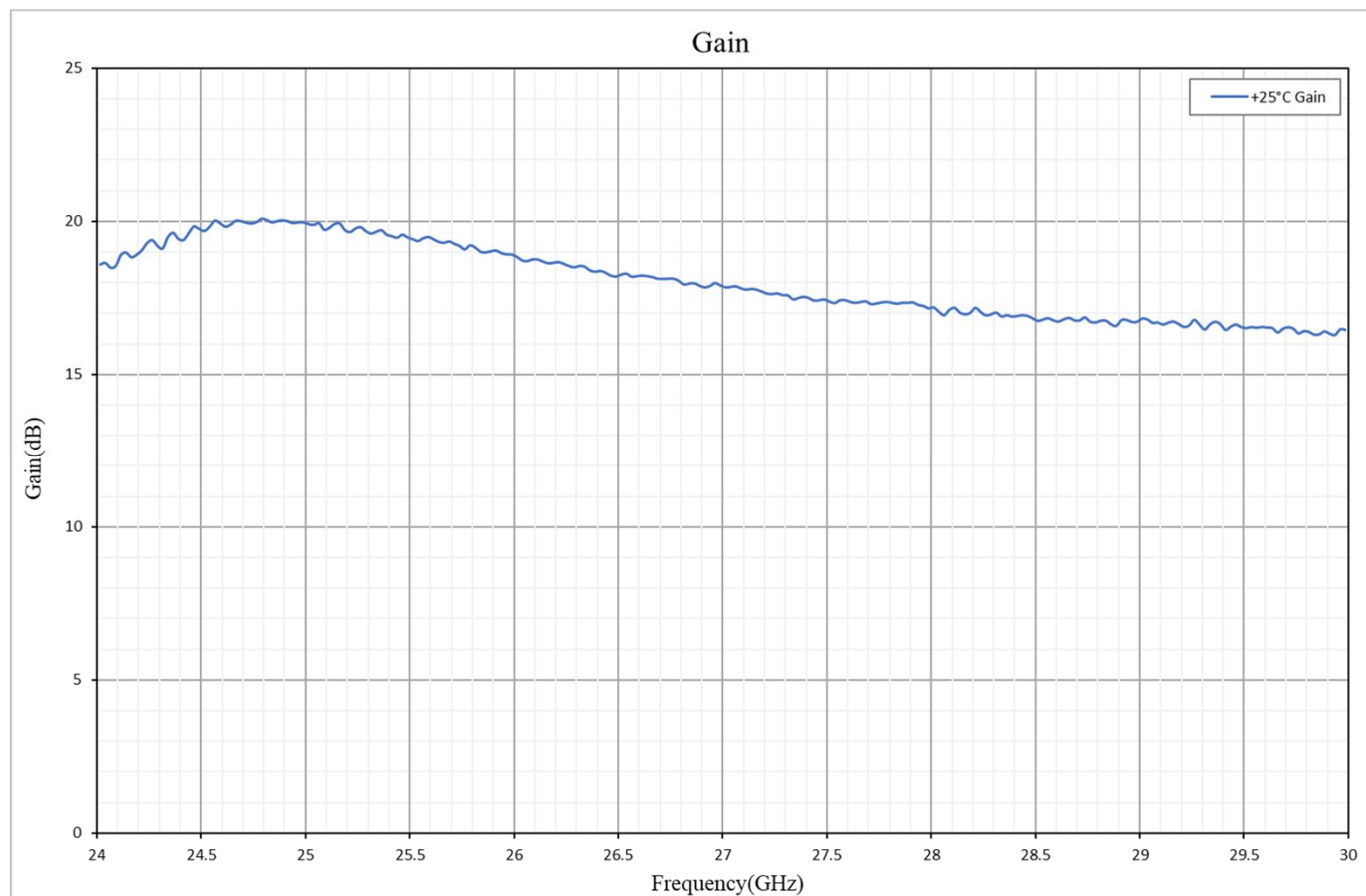
Parameters	Min.	Typ.	Max.	Unit
Frequency	24		30	GHz
Gain	16.3	18		dB
Gain variation over temperature		TBD		dB / $^\circ\text{C}$
Isolation	35.5	38		dB
Input Return Loss	3.4	9.1		dB
Output Return Loss	6.3	11.6		dB
Output P_{sat} @ 28 GHz		25		dBm
Output IP_3 @ 28 GHz ⁽¹⁾		32.6@-5dBm		dBm

Note:

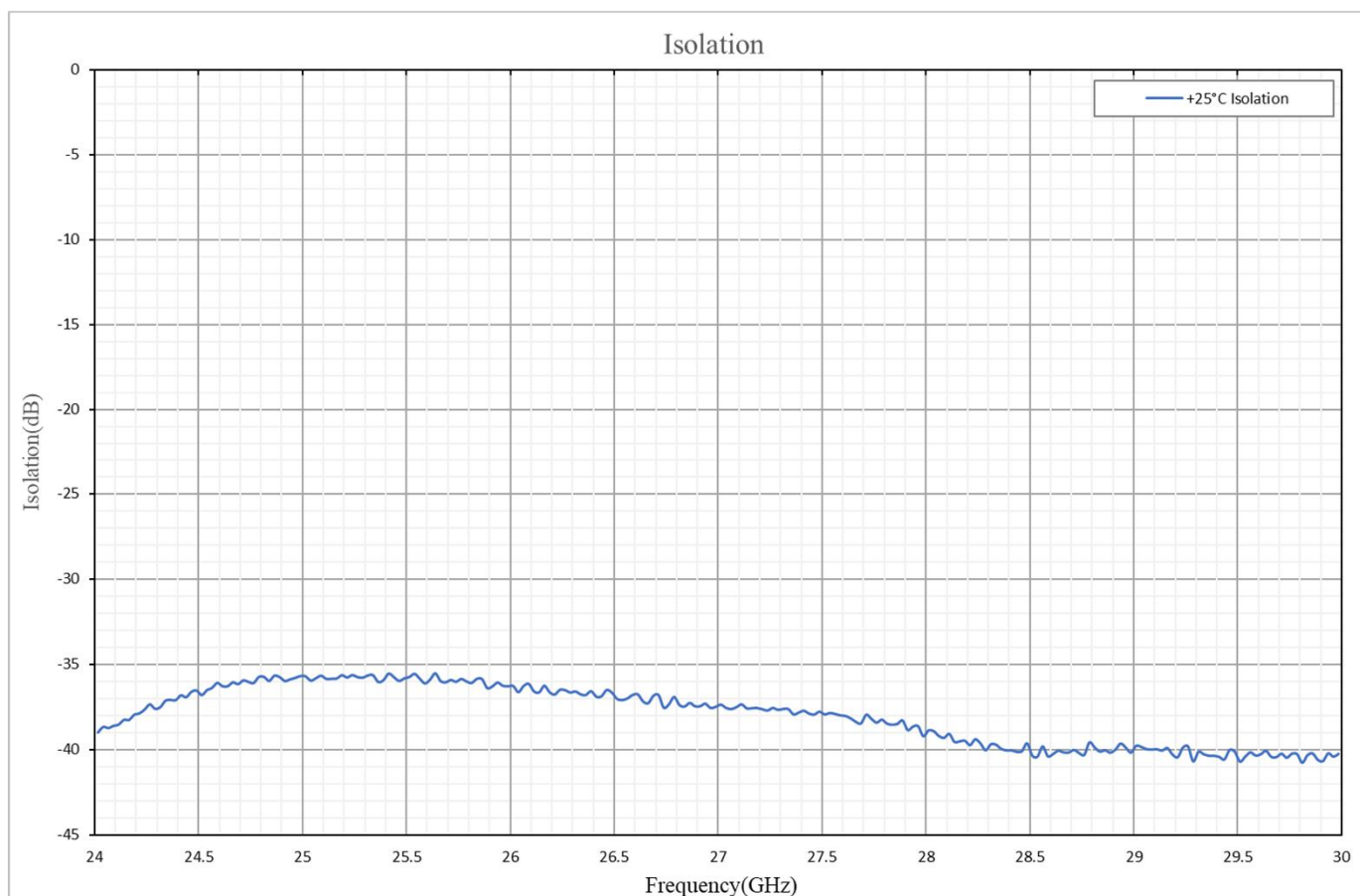
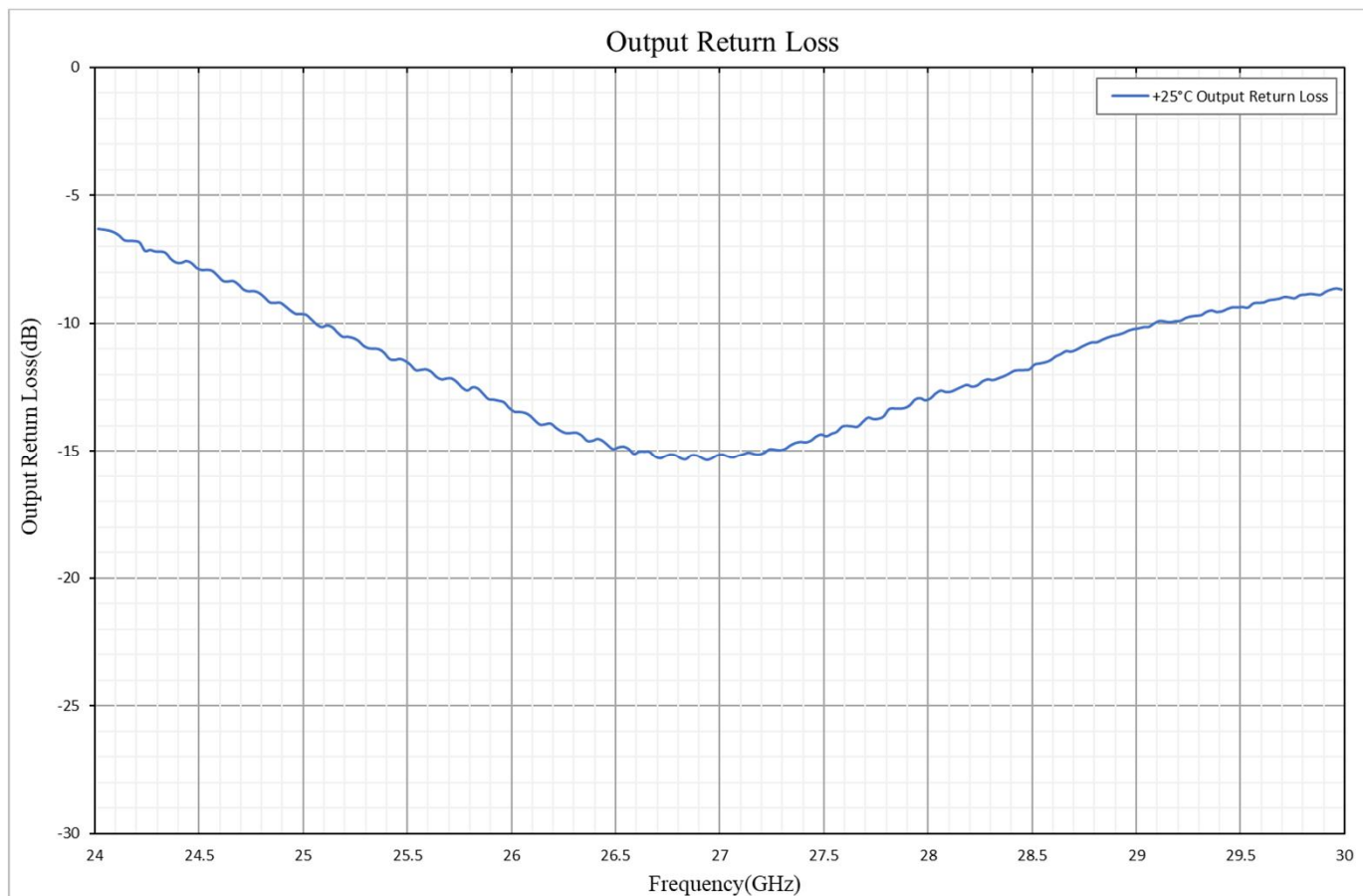
⁽¹⁾ 2 tone testing with 10 MHz spacing



Typical Performance

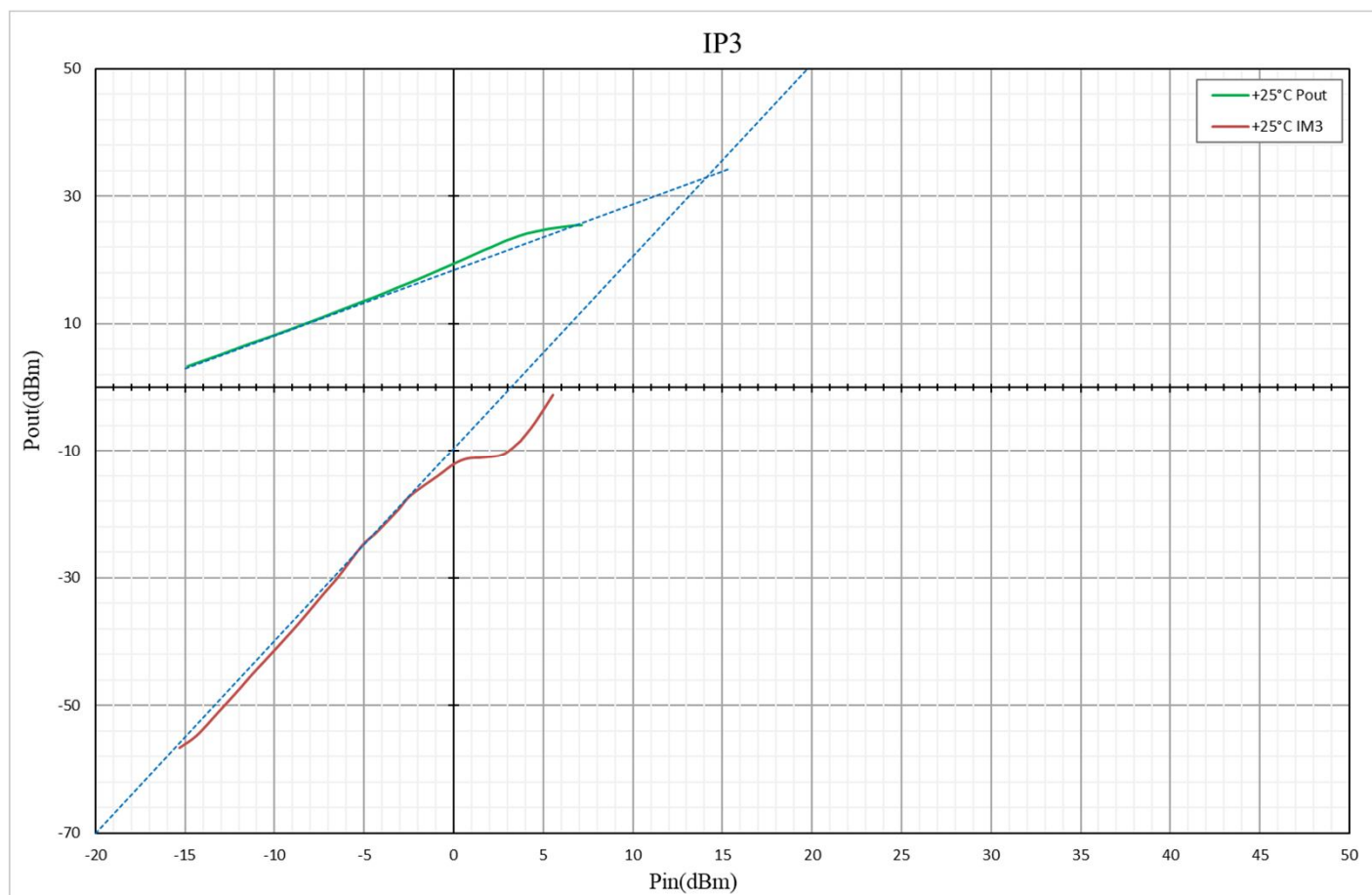
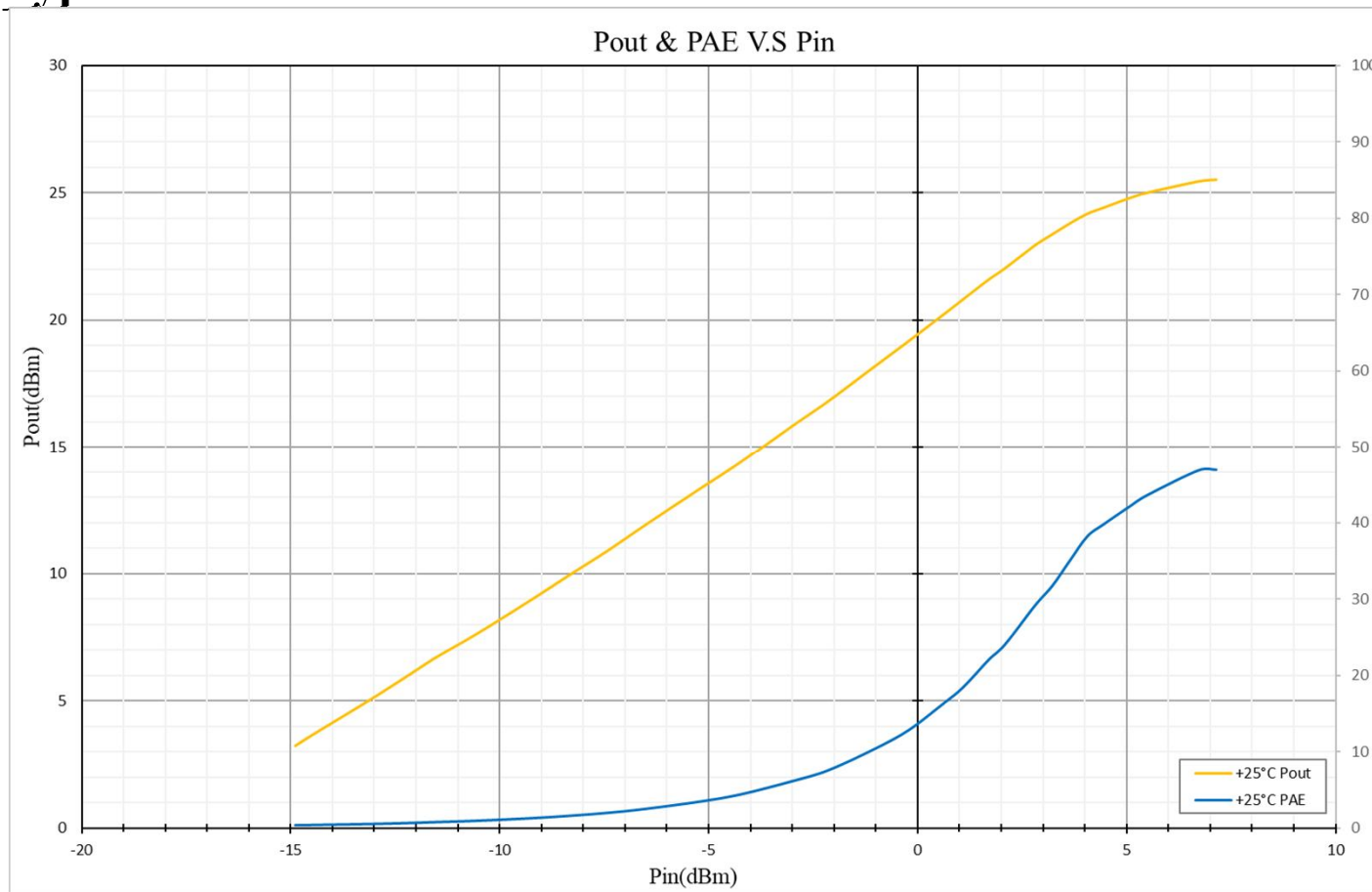


Typical Performance

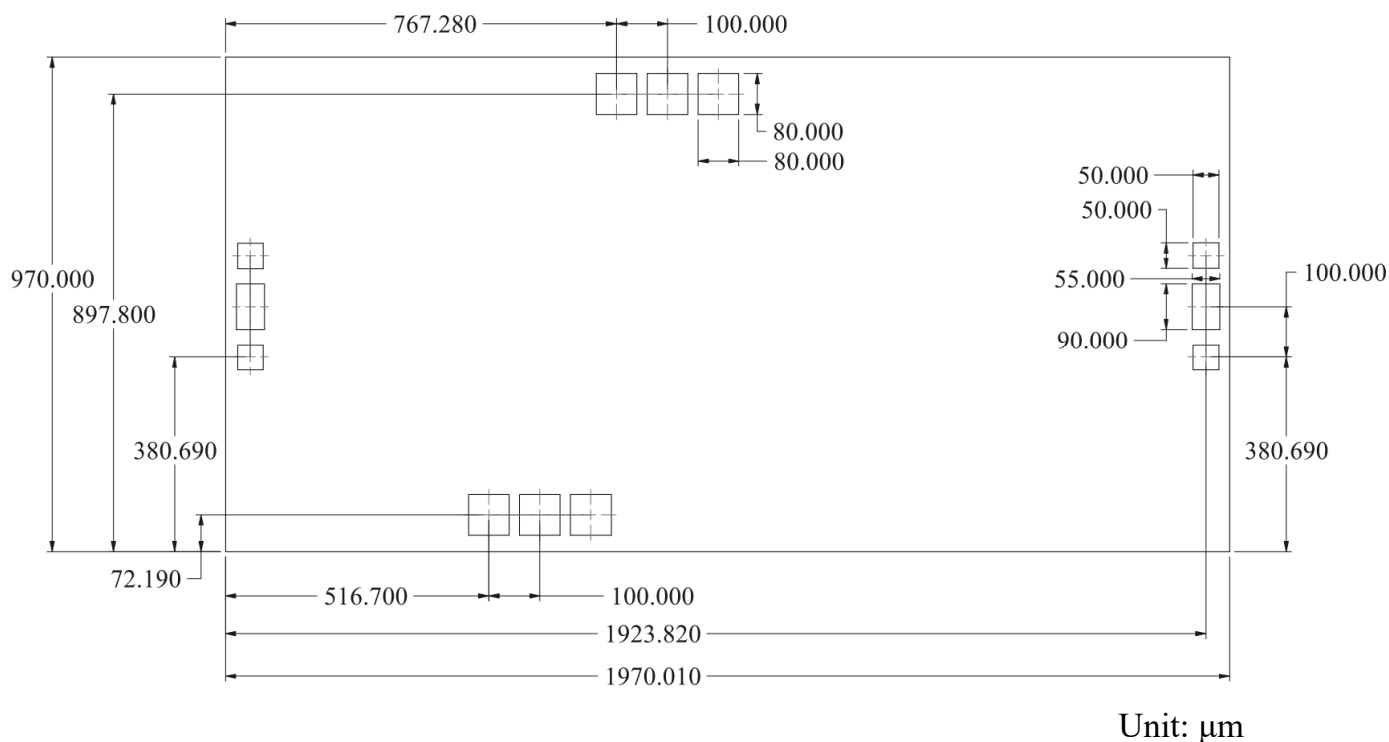




Typical Performance



Mechanical Information

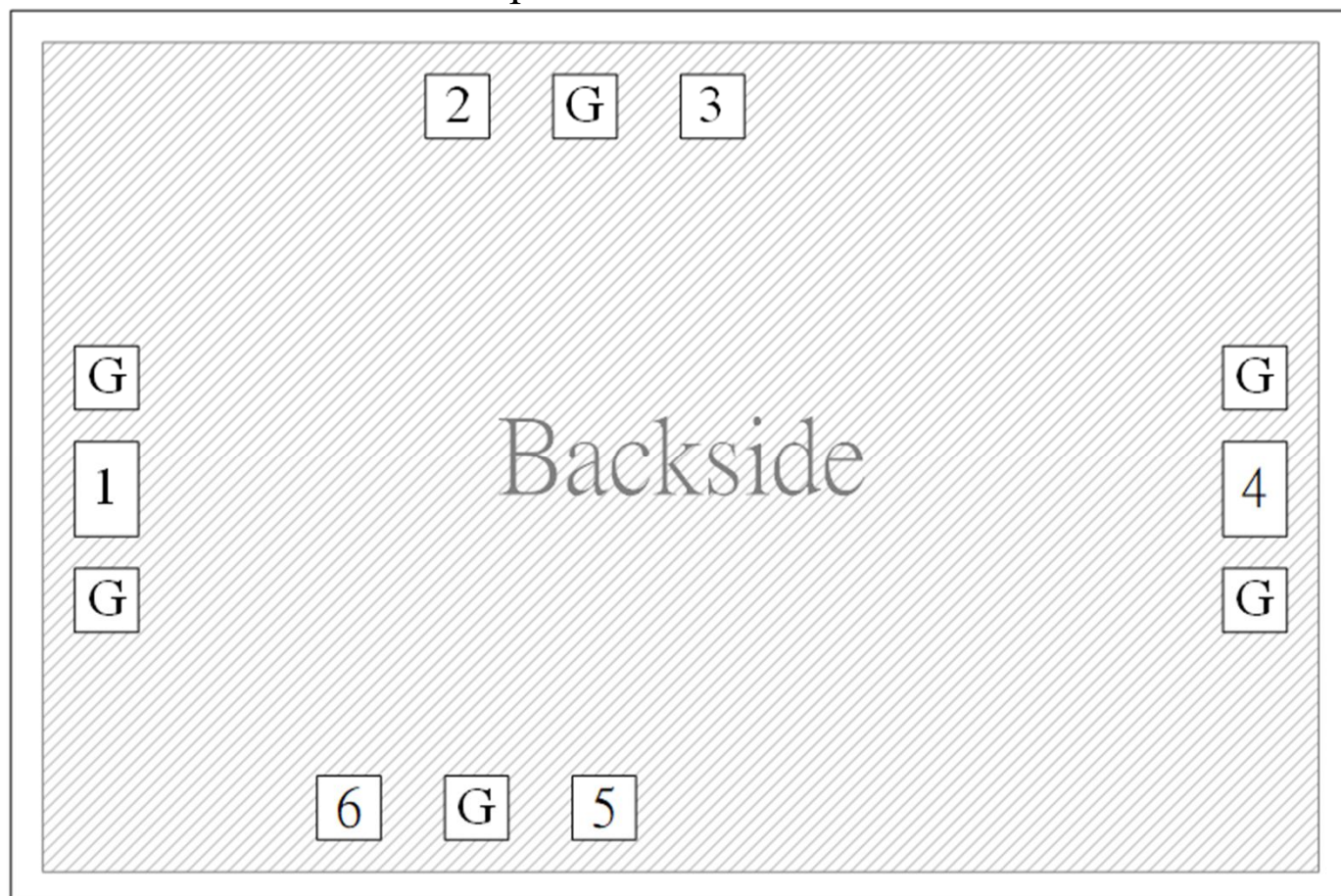


Notes:

1. RF Signal PAD size: $90 \mu\text{m} \times 55 \mu\text{m}$
2. RF Gnd PAD size: $50 \mu\text{m} \times 50 \mu\text{m}$
3. Drain and Gate PAD size: $80 \mu\text{m} \times 80 \mu\text{m}$
4. Die thickness: $100 \mu\text{m}$
5. Backside and bond pad metal: Gold
6. Backside is RF and DC ground

Pad Description

Pinout and Function Description



Pin Function Description

PIN#	Function	Description
1	RF_IN	This pin is matched to 50 Ω and built-in DC blocks
2	V _{d1}	Drain Voltage
3	V _{d2}	Drain Voltage
4	RF_OUT	This pin is matched to 50 Ω and built-in DC blocks
5	V _{g2}	Gate Voltage
6	V _{g1}	Gate Voltage
G	GND	Connect to RF and DC Ground
Backside	GND	Connect to RF and DC Ground

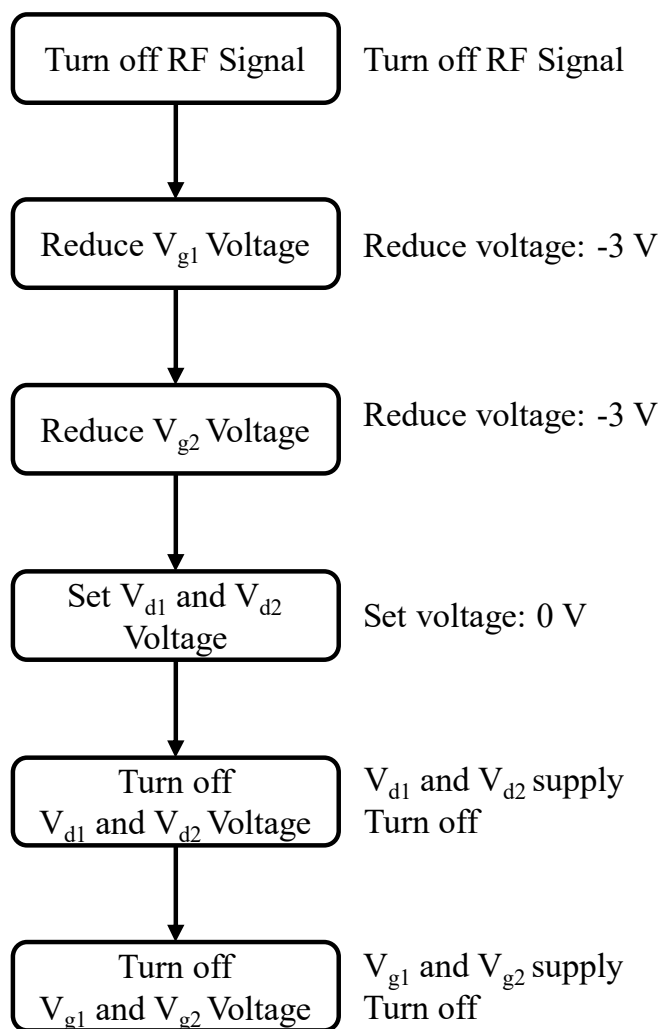
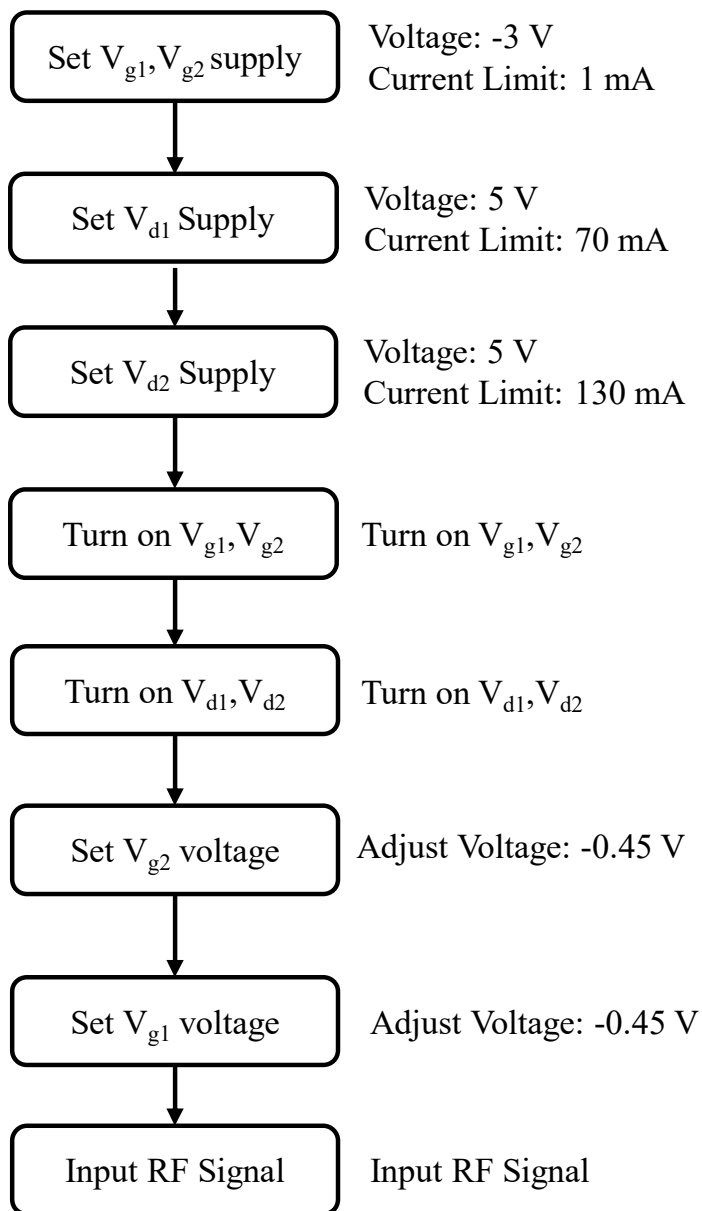
Application Information

Power-up Sequence

- 1) Set V_{g1}, V_{g2} voltage to -3 V, limit current to 1 mA
- 2) Set V_{d1} voltage to 5 V, limit current to 70 mA
- 3) Set V_{d2} voltage to 5 V, limit current to 130 mA
- 4) Turn on V_{g1}, V_{g2} supply
- 5) Turn on V_{d1}, V_{d2} supply
- 6) Adjust V_{g2} to -0.45V
- 7) Adjust V_{g1} to -0.45V
- 8) Apply RF signal

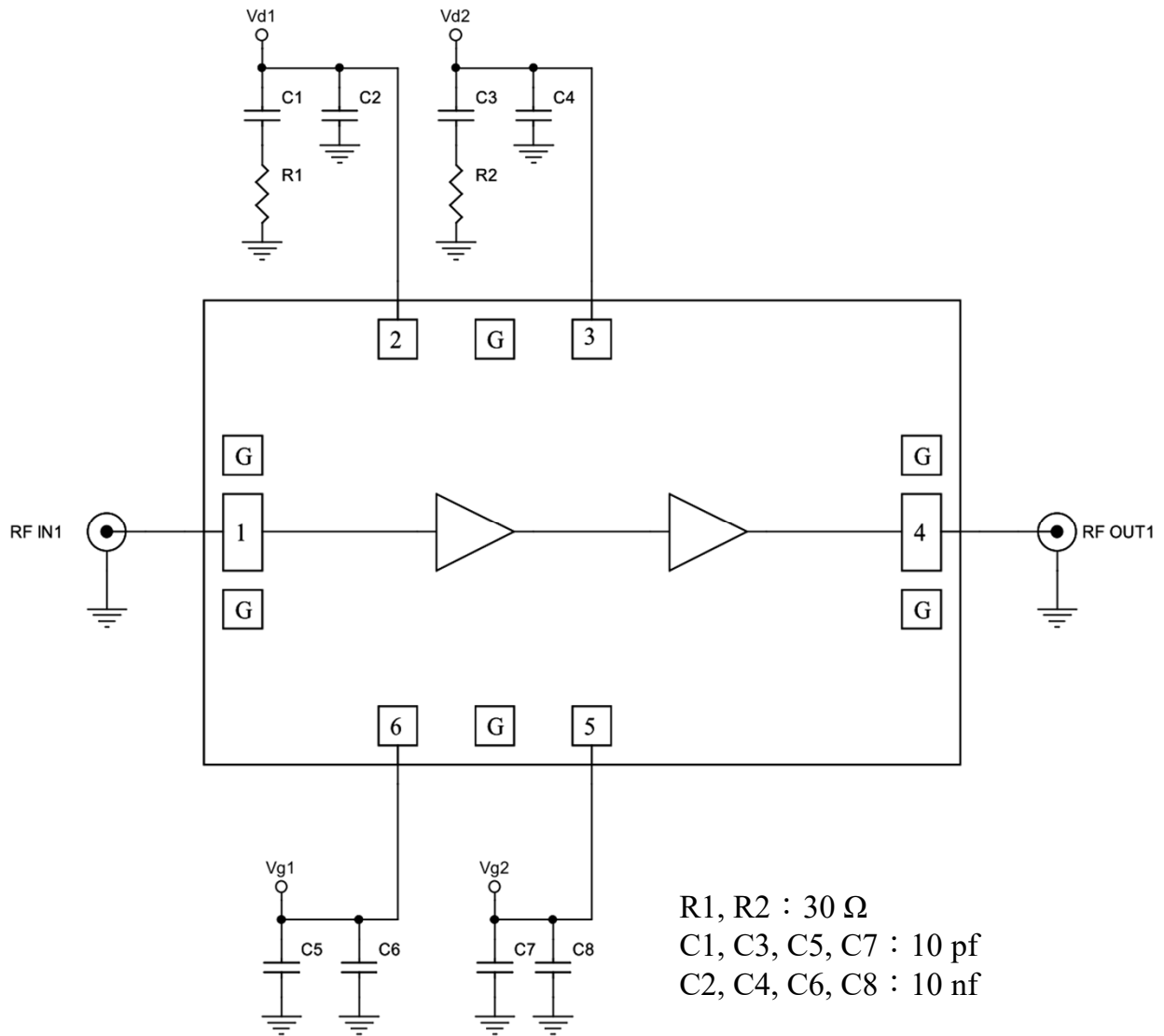
Power-down Sequence

- 1) Turn off RF signal
- 2) Reduce V_{g1} to -3 V, ensure $I_{d1} = 0$ mA
- 3) Reduce V_{g2} to -3 V, ensure $I_{d2} = 0$ mA
- 4) Set V_{d1}, V_{d2} voltage to 0 V
- 5) Turn off V_{d1}, V_{d2} supply
- 6) Turn off V_{g1}, V_{g2} supply



Application Information

Application Schematic



Application Information

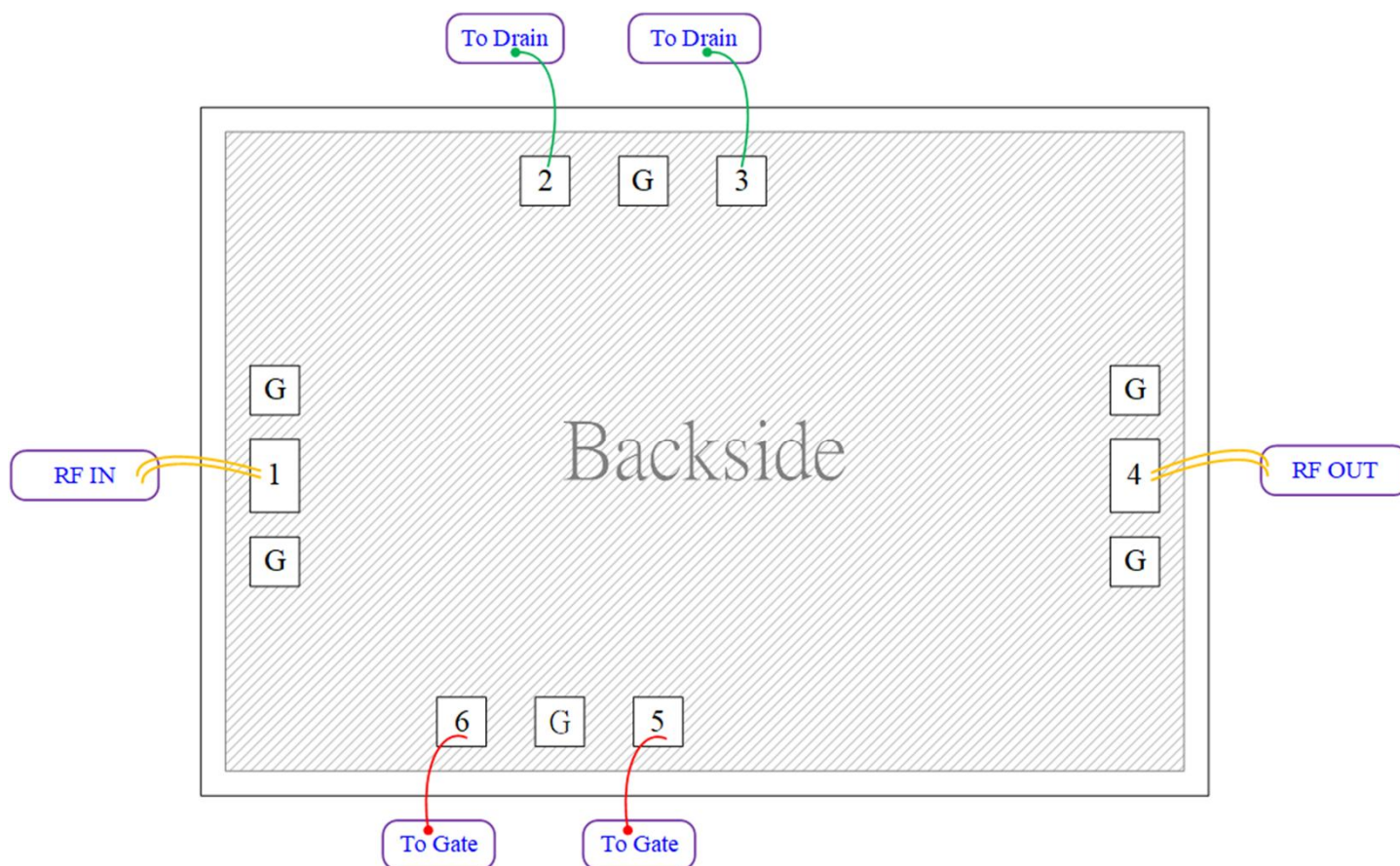
Assembly Guidelines

The URP5B98 backside pad is RF and DC ground, die assembly operations be performed under lamellar flow or in an environment maintained at Class 1000, or better. Die attach should be accomplished with electrically and thermally conductive epoxy only, eutectic attach is not recommended. The top surface of the semiconductor should be made planar to the adjacent RF transmission lines, and the RF decoupling capacitors placed in close proximity to the DC connections on chip.

RF connections should be made as short as possible to reduce the inductive effect of the bond wire.

This chip thickness is 100 μm and should be handled by the sides of the die or with a custom collet. Do not make contact directly with the die surface as this will damage the monolithic circuitry. Handle with care.

Assembly Diagram



Note: GaAs pHEMT dies are susceptible to chipping and cracking if not properly been handled, causing reliability concerns.



Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices

ESD Precaution:

Protection must be afforded for the personnel, equipment, and working environment. Employees handling die must wear static dissipative wrist straps. Both the worktables and floors (or local floor mats) must be grounded to allow for static dissipation as well. Work-in-process and finished goods must be stored in an ESD protected environment. Static induced failures are often latent. The damage may not be obvious at the time of exposure of the die to ESD. Therefore, it is a good practice to insure that both the working environment and the handling techniques are compliant with the requirements for handling devices which are sensitive to ESD.

RoHS Compliance

RoHS:	UltrabandTech defines “RoHS” to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, “RoHS” products are suitable for use in specified lead-free processes. UltrabandTech may reference these types of products as "Pb-Free".
RoHS Exempt:	UltrabandTech defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green:	UltrabandTech defines “Green” to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000 ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000 ppm threshold requirement.

Important Notice

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