# URP5B95 mmWave PA

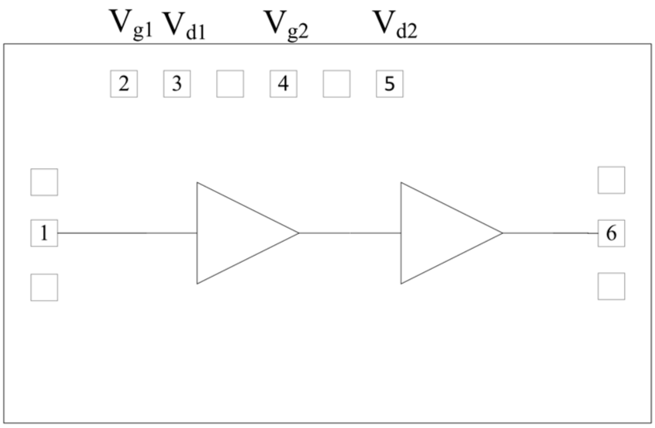
## Product Overview

The URP5B95 is a 1W MMIC integrated the mmWave PA in die form, which is designed by using 0.15 μm GaAs pHEMT devices in a compact die size with excellent performance.

## Key Features

- 26 – 30 GHz frequency range
- Gain：18.3 dB
- Gain flatness： ± 0.95 dB
- $P_{1dB}$ ：30 dBm
- $P_{sat}$ ：30.2 dBm
- PAE ：50%
- high OIP3 ：37 dBm
- Die Size：2665 μm × 1590 μm

## Functional Block Diagram




## Application

- 5G FR2 Antenna Modules
- FWA
- Satcom
- Radar

## Ordering Information

| Part Number | Package |
|---|---|
| URP5B95 | Die |

## Absolute Maximum Ratings

| Parameters | Rating | Unit |
|---|---|---|
| DC Drain Voltage | 10 | V |
| CW Incident Power | >15 | dBm |
| Operating temperature | -40˚C to +85˚C | ˚C |
| Storage Temperature | -65˚C to +150˚C | ˚C |

## Recommended Operating Conditions

| Parameter | Value | Unit |
|---|---|---|
| $V_{d1}$, $V_{d2}$ | 5 | V |
| $V_{g1}$ | -0.55 | V |
| $I_{d1}$ (Quiescent) | 87 | mA |
| $V_{g2}$ | -0.5 | V |
| $I_{d2}$ (Quiescent) | 215 | mA |

# Electrical Specifications ($T_A$ = 25 ˚C, $V_{d1}$ ,$V_{d2}$= 5 V, $I_{d1}$ = 87 mA , $I_{d2}$ = 215 mA, $Z_0$ = 50 Ω)

| Parameters | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Frequency | 26 | | 30 | GHz |
| Gain | 17.5 | 18.3 | | dB |
| Gain flatness | | ±0.95 | | dB |
| Gain variation over temperature | | TBD | | dB / ˚C |
| Isolation | 37.9 | 40 | | dB |
| Input Return Loss | 4.6 | 8.5 | | dB |
| Output Return Loss | 5.8 | 19.4 | | dB |
| Output $P_{1dB}$@ 28 GHz | | 30 | | dBm |
| Output $P_{sat}$ @ 28 GHz | | 30.2 | | dBm |
| Output $IP_3$ @ 28 GHz (1) | | 37.7@0dBm | | dBm |

Note:
(1) 2 tone testing with 10 MHz spacing



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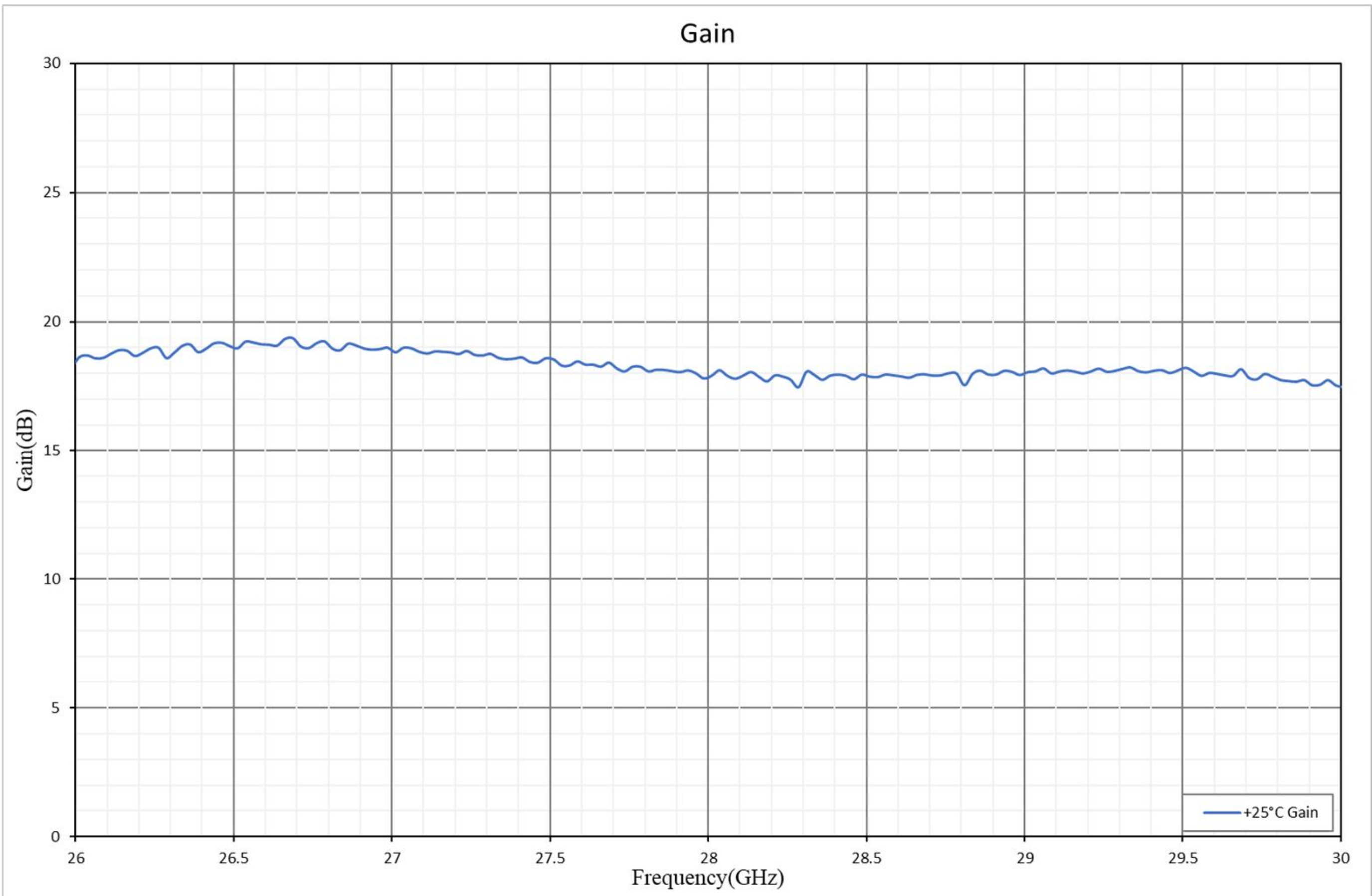
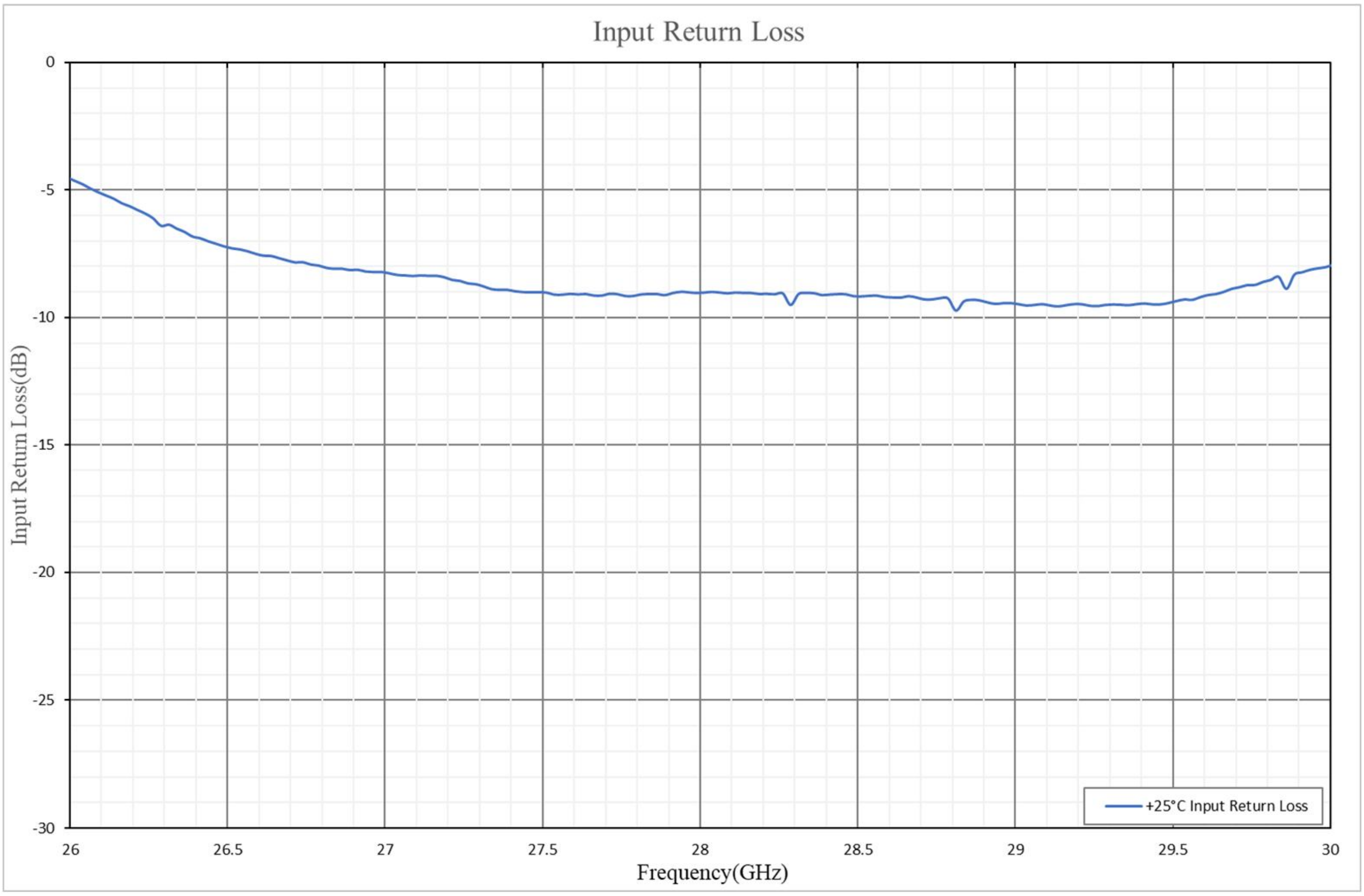
# Typical Performance



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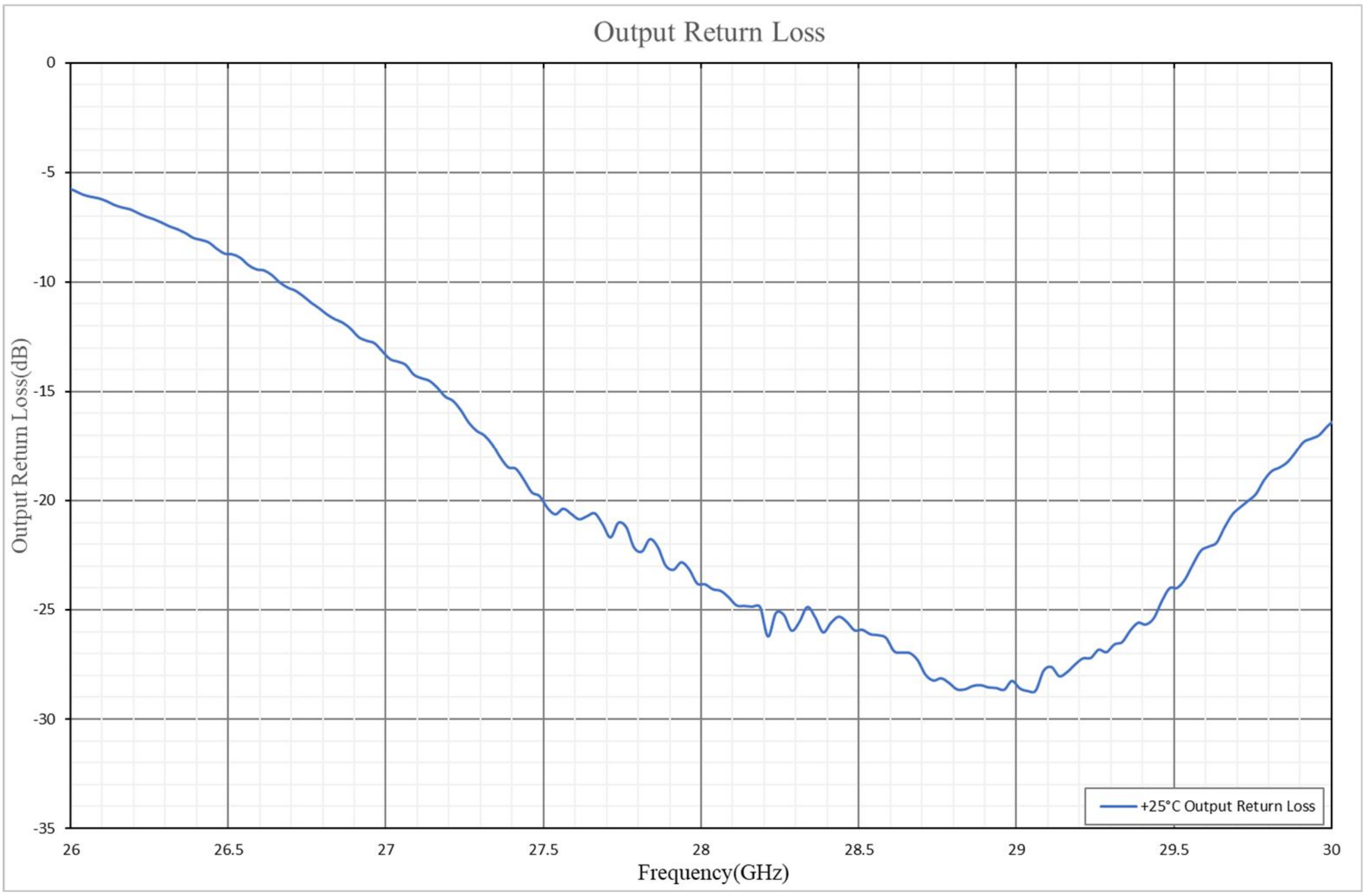


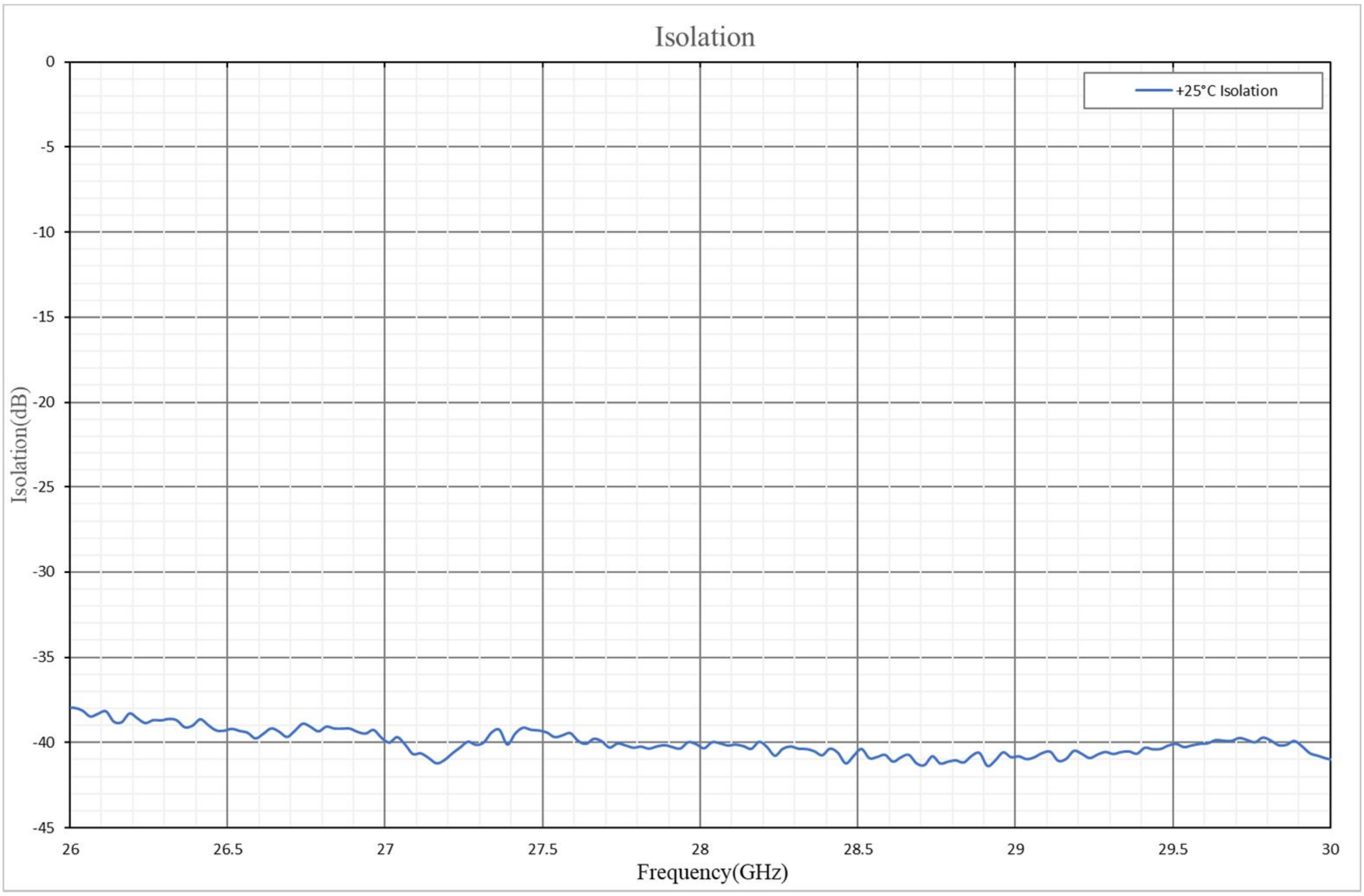




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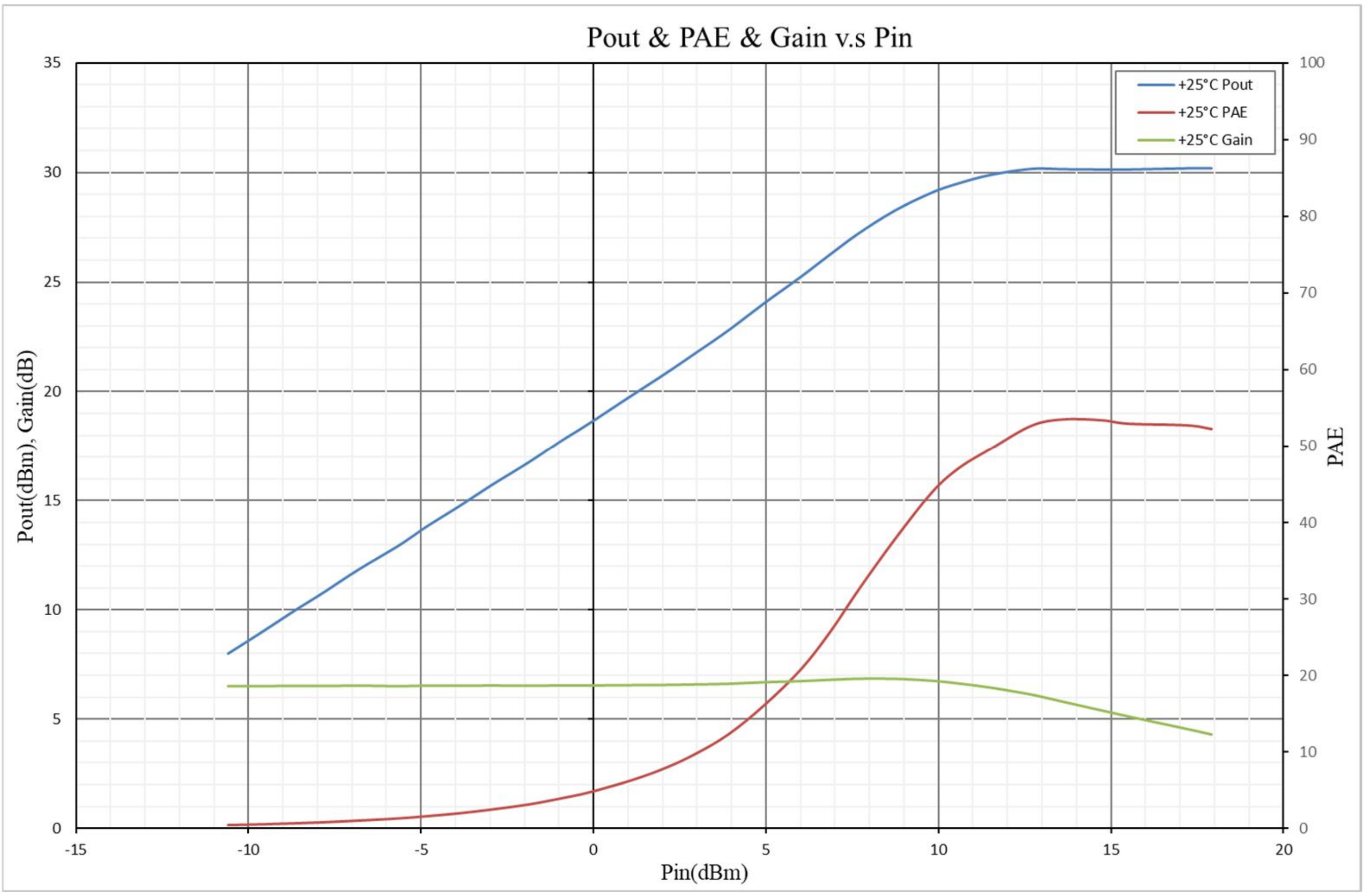


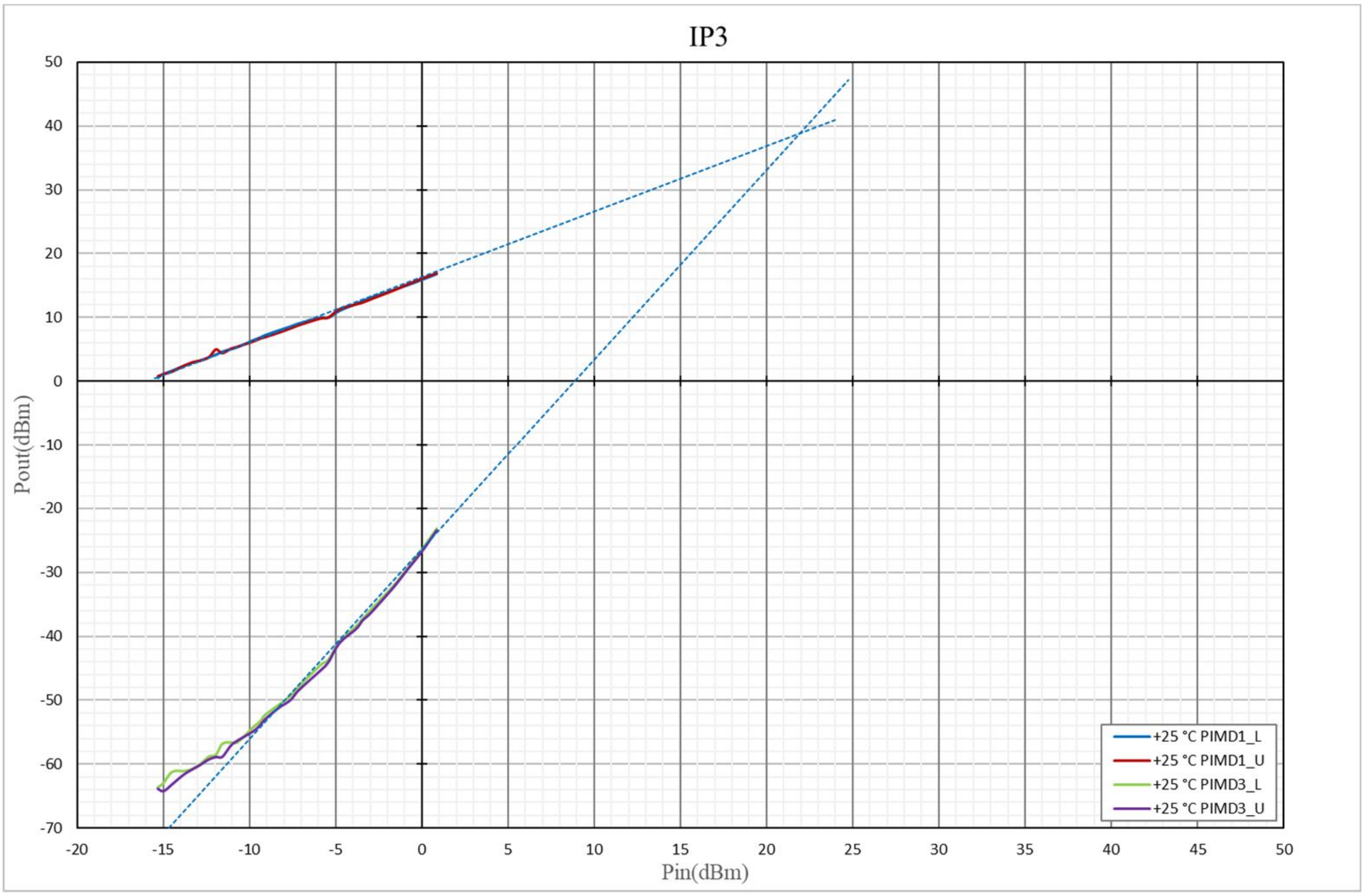




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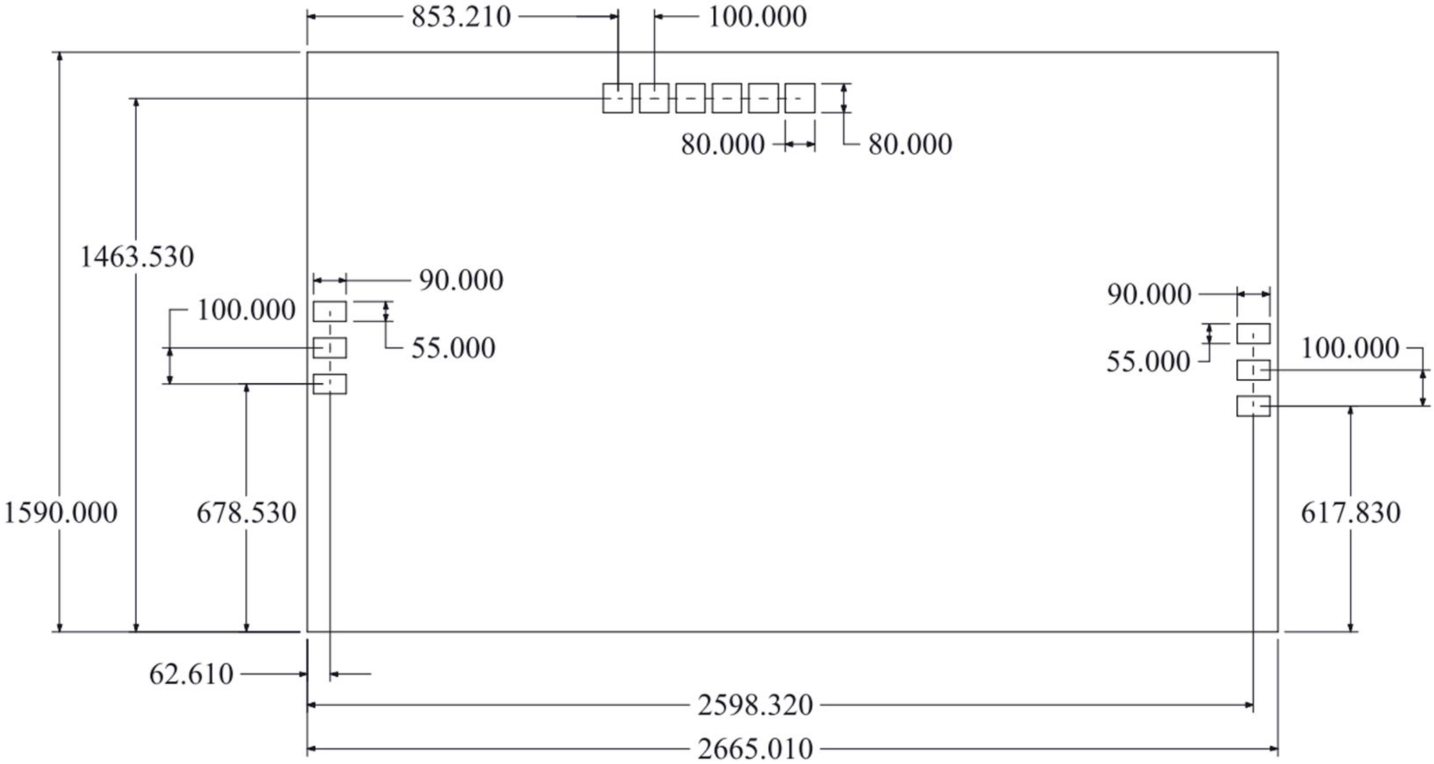
# Mechanical Information




Unit: µm

Notes:

1.RF Signal PAD size: 90 µm × 55 µm

2.Drain and Gate PAD size: 80 µm × 80 µm

3.Die thickness: 100 µm

4.Backside and bond pad metal: Gold

5.Backside is RF and DC ground



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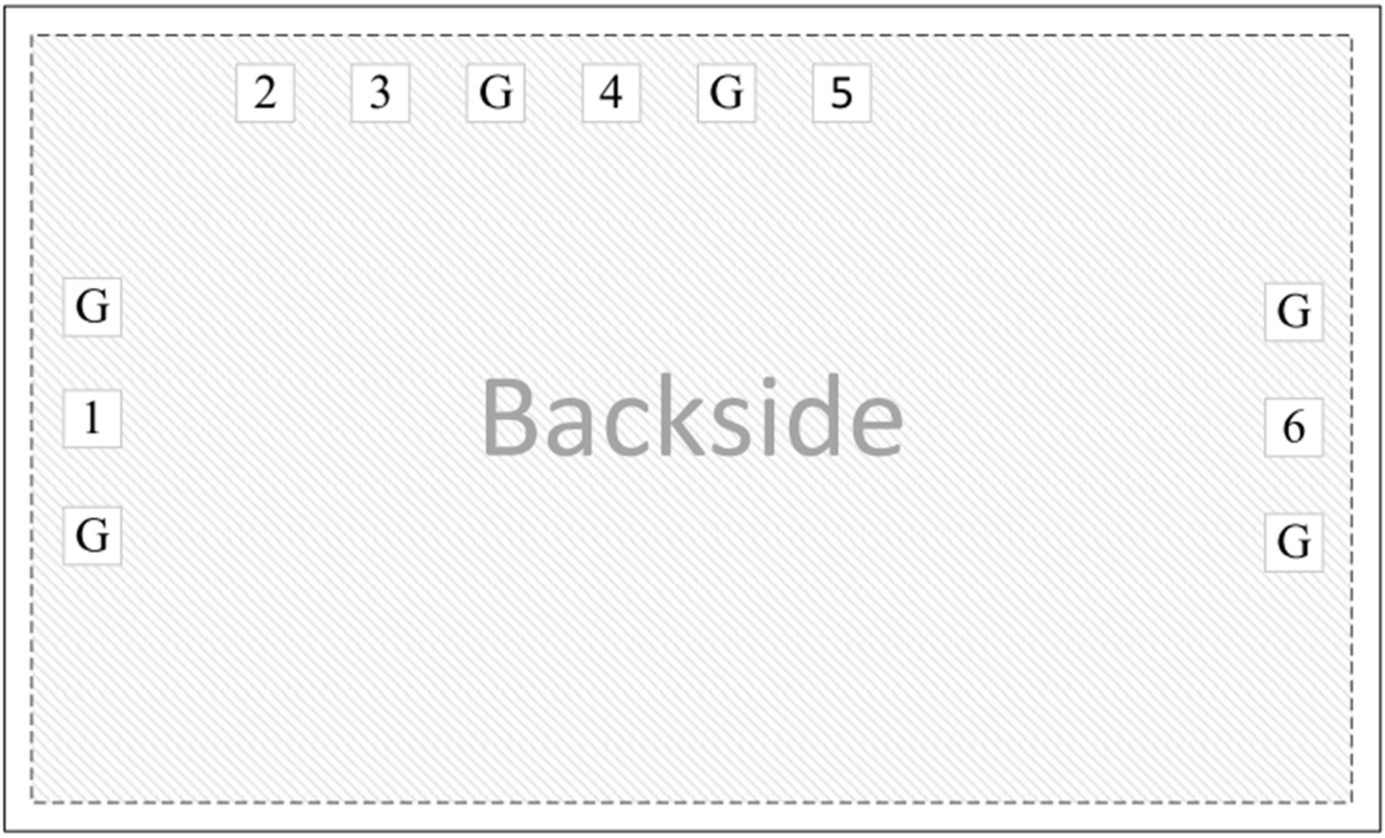
# Pad Description

## Pinout and Function Description




## Pin Function Description

| PIN# | Function | Description |
|---|---|---|
| 1 | RF_IN | This pin is matched to 50 Ω and built-in DC blocks |
| 2 | $V_{g1}$ | Gate Voltage |
| 3 | $V_{d1}$ | Drain Voltage |
| 4 | $V_{g2}$ | Gate Voltage |
| 5 | $V_{d2}$ | Drain Voltage |
| 6 | RF_OUT | This pin is matched to 50 Ω and built-in DC blocks |
| G | GND | Connect to RF and DC Ground |
| Backside | GND | Connect to RF and DC Ground |

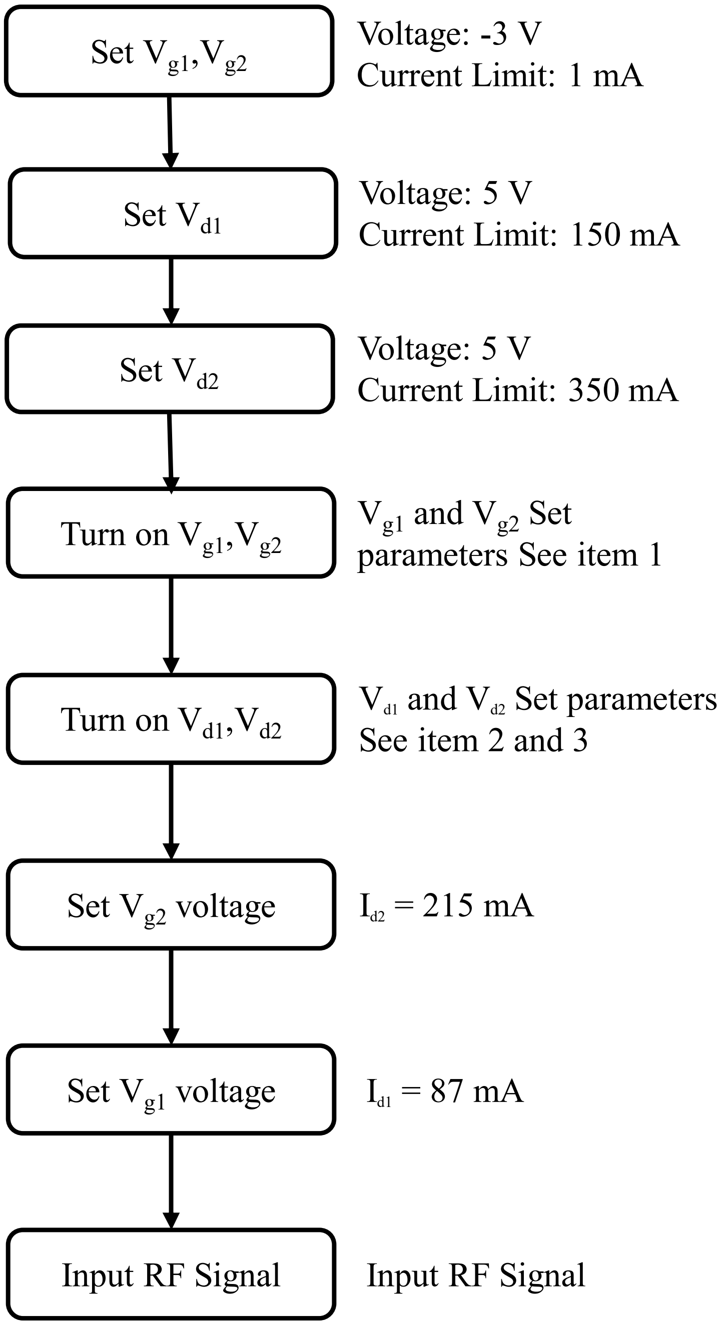
# Application Information

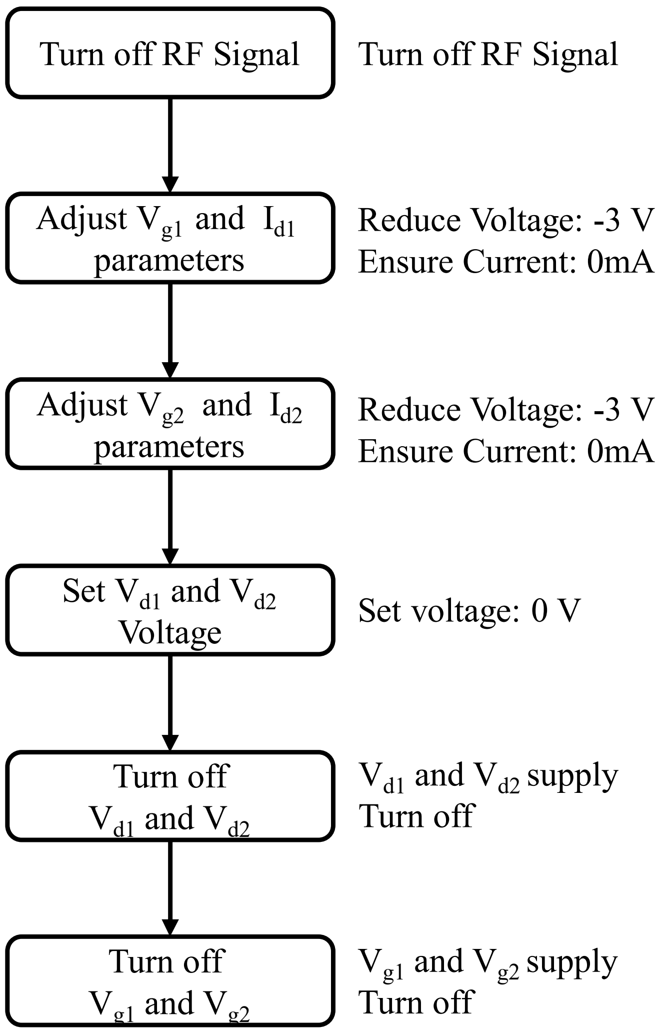
## Power-up Sequence

1) Set $V_{g1}$,$V_{g2}$ voltage to -3 V, limit current to 1 mA
2) Set $V_{d1}$ voltage to 5 V, limit current to 150 mA
3) Set $V_{d2}$ voltage to 5 V, limit current to 350 mA
4) Turn on $V_{g1}$,$V_{g2}$ supply
5) Turn on $V_{d1}$,$V_{d2}$ supply
6) Adjust Vg2 more positive until $I_{d2}$ = 215 mA
7) Adjust Vg1 more positive until $I_{d1}$ = 87 mA
8) Apply RF signal

## Power-down Sequence

1) Turn off RF signal
2) Reduce $V_{g1}$ to -3 V, ensure $I_{d1}$ = 0 mA
3) Reduce $V_{g2}$ to -3 V, ensure $I_{d2}$ = 0 mA
4) Set $V_{d1}$,$V_{d2}$ voltage to 0 V
5) Turn off $V_{d1}$,$V_{d2}$ supply
6) Turn off $V_{g1}$,$V_{g2}$ supply



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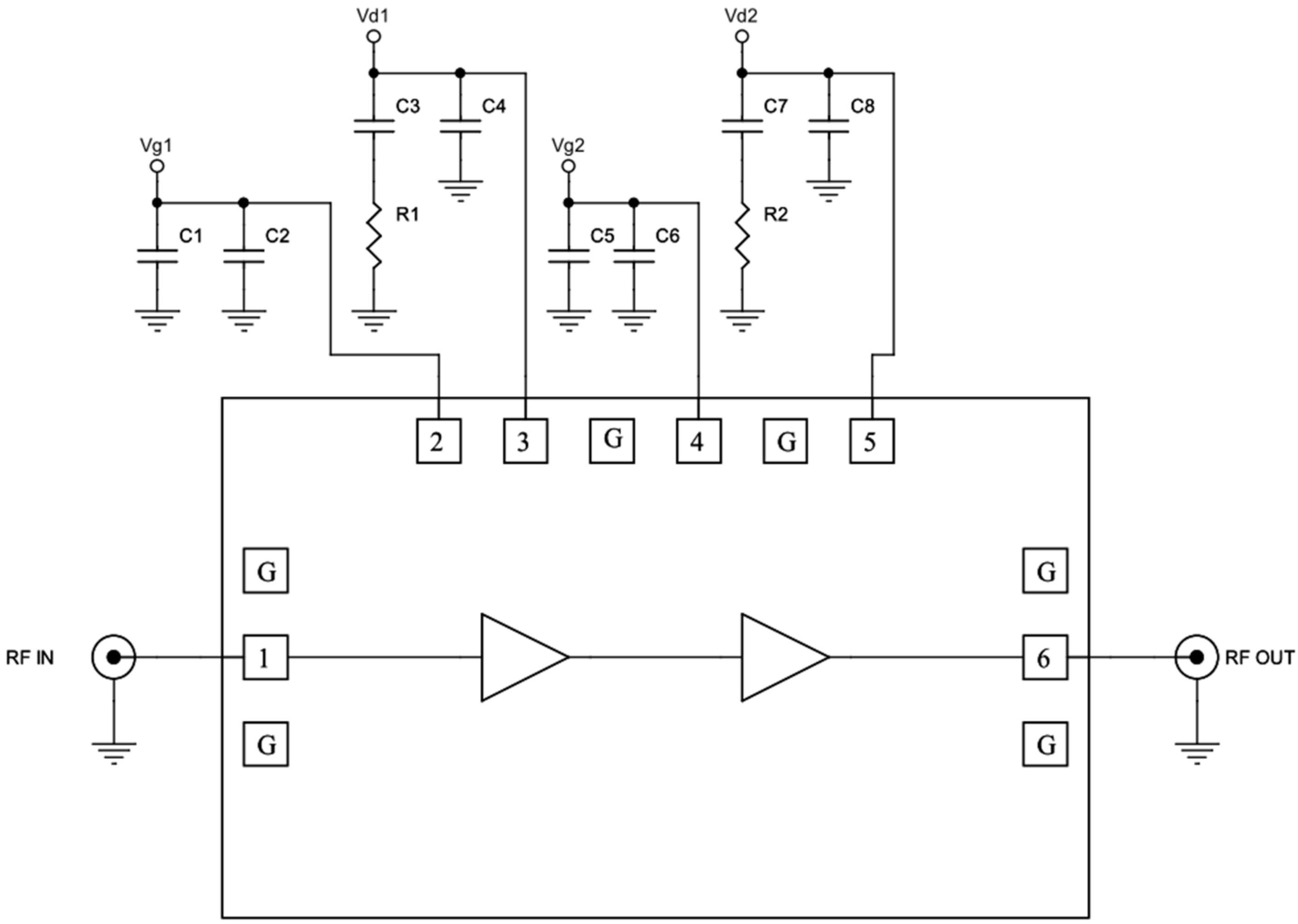
# Application Information

## Application Schematic




R1,R2: 30 Ω

C1,C3,C5,C7: 10 nF

C2,C4,C6,C8: 10 pF



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# Application Information

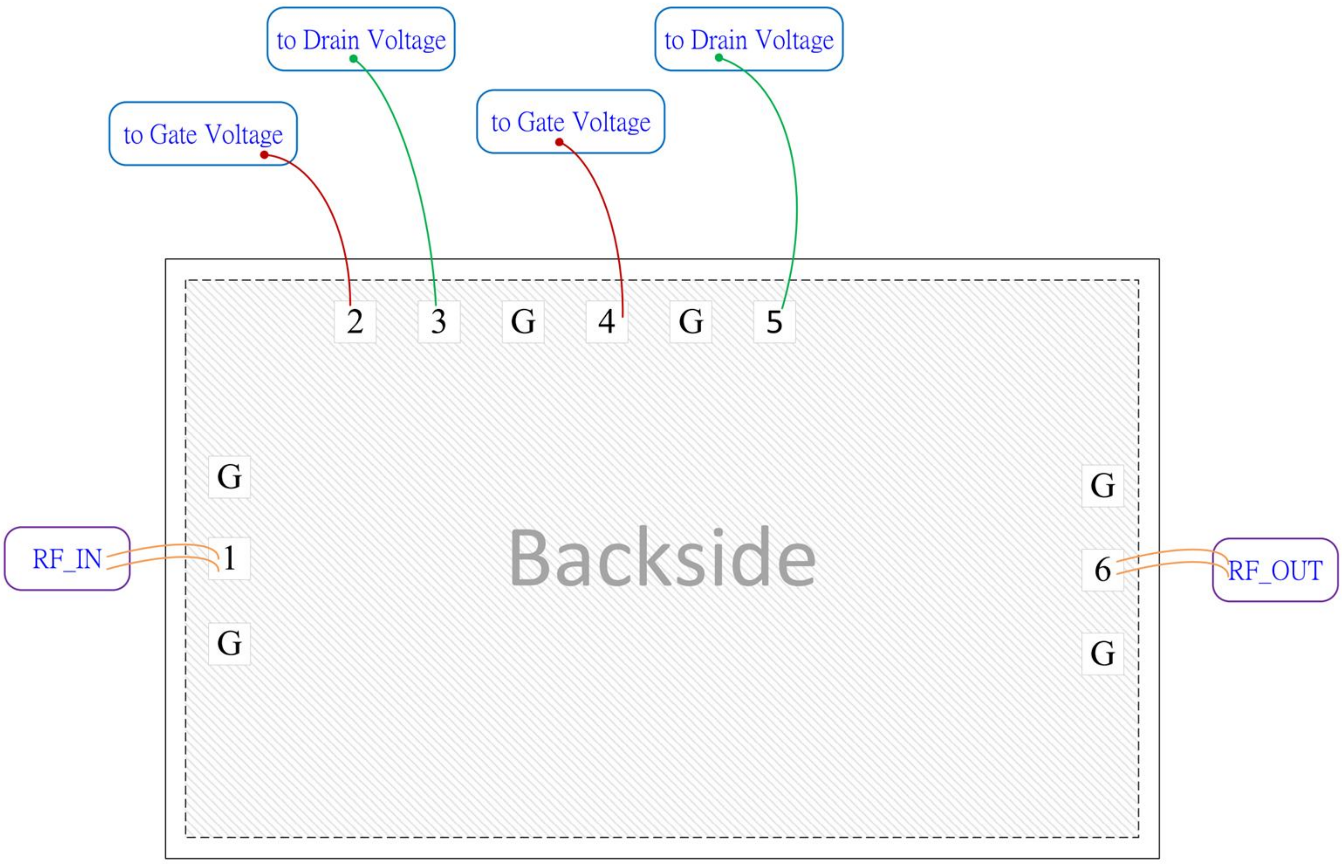
## Assembly Guidelines

The URP5B95 backside pad is RF and DC ground, die assembly operations be performed under lamellar flow or in an environment maintained at Class 1000, or better. Die attach should be accomplished with electrically and thermally conductive epoxy only, eutectic attach is not recommended. The top surface of the semiconductor should be made planar to the adjacent RF transmission lines, and the RF decoupling capacitors placed in close proximity to the DC connections on chip.

RF connections should be made as short as possible to reduce the inductive effect of the bond wire.

This chip thickness is 100 µm and should be handled by the sides of the die or with a custom collet. Do not make contact directly with the die surface as this will damage the monolithic circuitry. Handle with care.

## Assembly Diagram




Note: GaAs pHEMT dies are susceptible to chipping and cracking if not properly been handled, causing reliability concerns.



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## Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices

## ESD Precaution:

Protection must be afforded for the personnel, equipment, and working environment. Employees handling die must wear static dissipative wrist straps. Both the worktables and floors (or local floor mats) must be grounded to allow for static dissipation as well. Work-in-process and finished goods must be stored in an ESD protected environment. Static induced failures are often latent. The damage may not be obvious at the time of exposure of the die to ESD. Therefore, it is a good practice to insure that both the working environment and the handling techniques are compliant with the requirements for handling devices which are sensitive to ESD.

## RoHS Compliance

| | |
|---|---|
| RoHS: | UltrabandTech defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. UltrabandTech may reference these types of products as "Pb-Free". |
| RoHS Exempt: | UltrabandTech defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption. |
| Green: | UltrabandTech defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000 ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000 ppm threshold requirement. |

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