

Product Overview

The URP5A98 is an OP_{1dB} of 26 dBm MMIC integrated the mmWave PA in die form, which is designed by using 0.15 μm GaAs pHEMT devices in a compact die size with excellent performance.

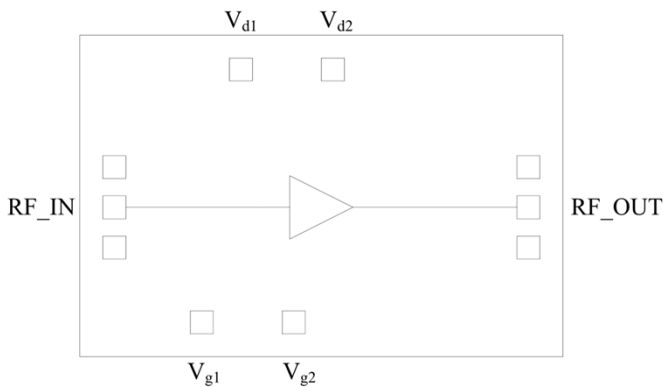
Key Features

- 24 – 30 GHz frequency range
- Gain : 17 dB
- Gain flatness : ± 0.98 dB
- OP_{1dB} : 26 dBm
- PAE : 30%
- OIP3 : 31.7 dBm
- Die Size : 1770 μm \times 1270 μm

Application

- 5G FR2 Antenna Modules
- FWA
- Satcom
- Radar

Functional Block Diagram



Ordering Information

Part Number	Package
URP5A98	Die

Absolute Maximum Ratings

Parameters	Rating	Unit
DC Drain Voltage	10	V
CW Incident Power	>12	dBm
Operating temperature	-40°C to +85°C	°C
Storage Temperature	-65°C to +150°C	°C

Recommended Operating Conditions

Parameter	Value	Unit
V_{d1}, V_{d2}	6	V
V_{g1}	-0.55	V
I_{d1} (Quiescent)	36.6	mA
V_{g2}	-0.5	V
I_{d2} (Quiescent)	56.8	mA



Electrical Specifications ($T_A = 25\text{ }^\circ\text{C}$, $V_{d1}, V_{d2} = 5\text{ V}$, $V_{g1} = -0.55\text{ V}$, $V_{g2} = -0.5\text{ V}$, $Z_0 = 50\text{ }\Omega$)

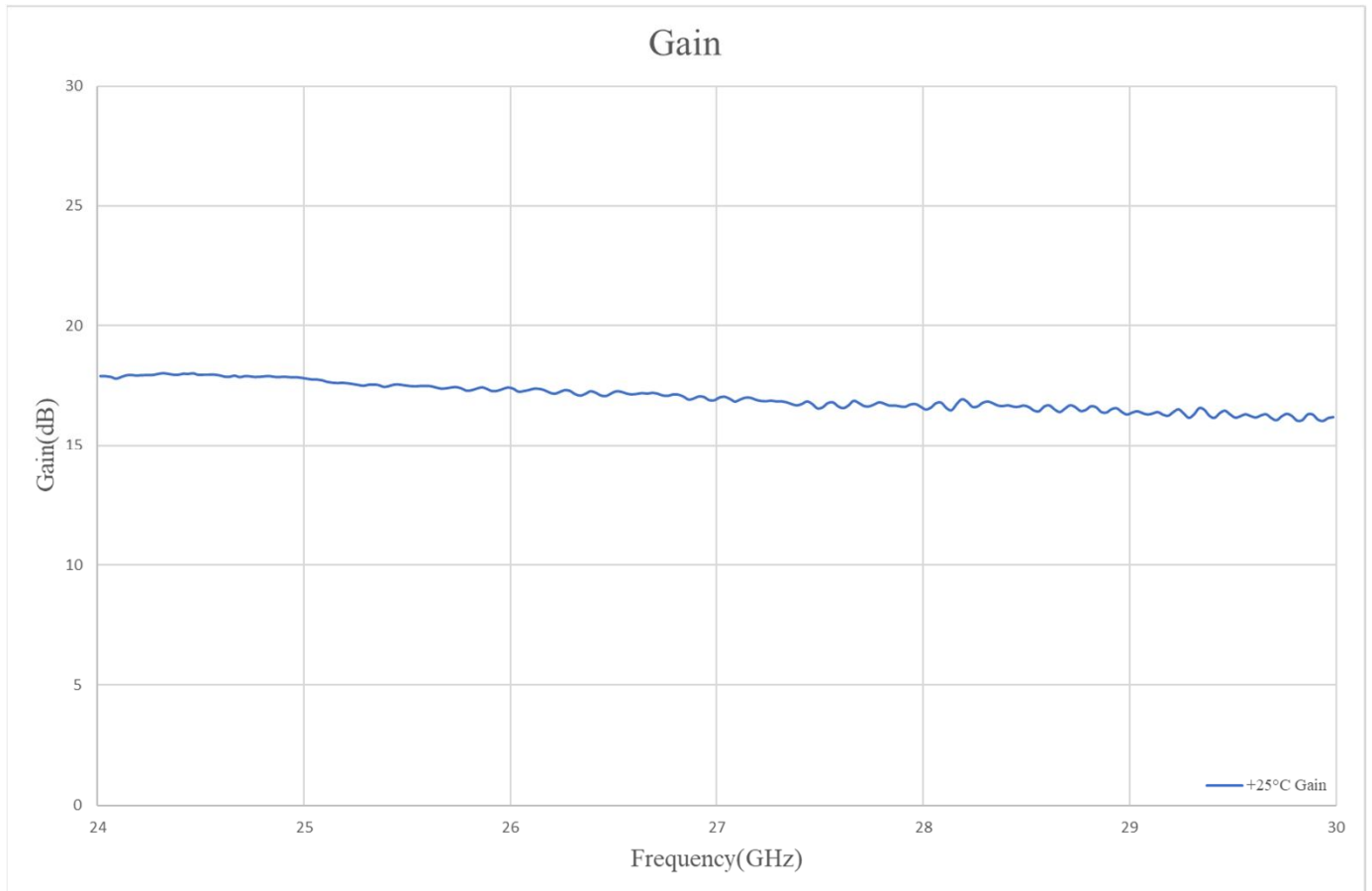
Parameters	Min.	Typ.	Max.	Unit
Frequency	24		30	GHz
Gain	16	17		dB
Gain flatness		± 0.98		dB
Gain variation over temperature				dB / $^\circ\text{C}$
Isolation	40.3	47.2		dB
Input Return Loss	10.1	15.2		dB
Output Return Loss	11.1	15.9		dB
Output P_{1dB} @ 28 GHz		26		dBm
Output IP_3 @ 28 GHz ⁽¹⁾		31.7@0 dBm		dBm

Note:

(1) 2 tone testing with 10 MHz spacing

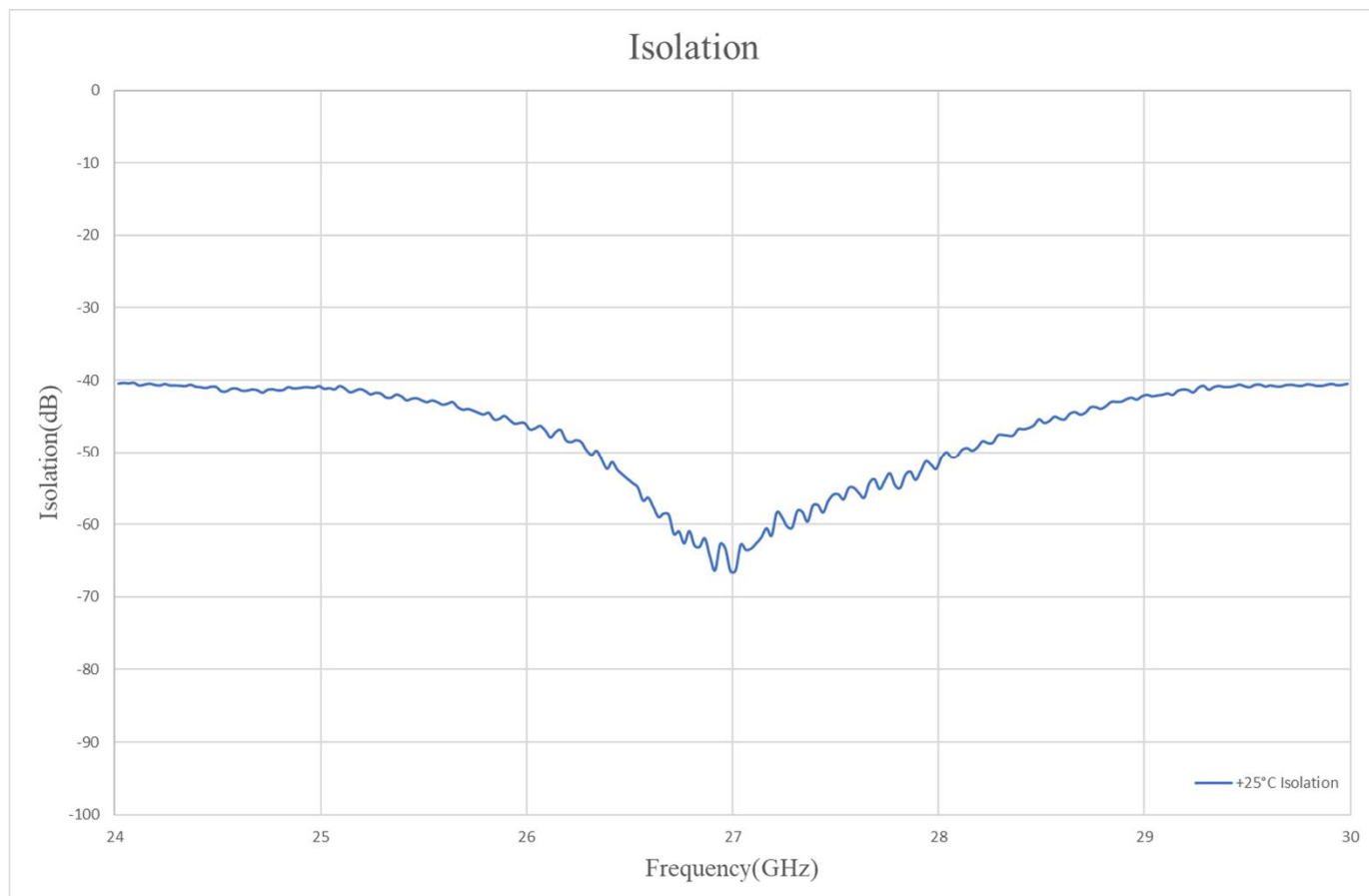
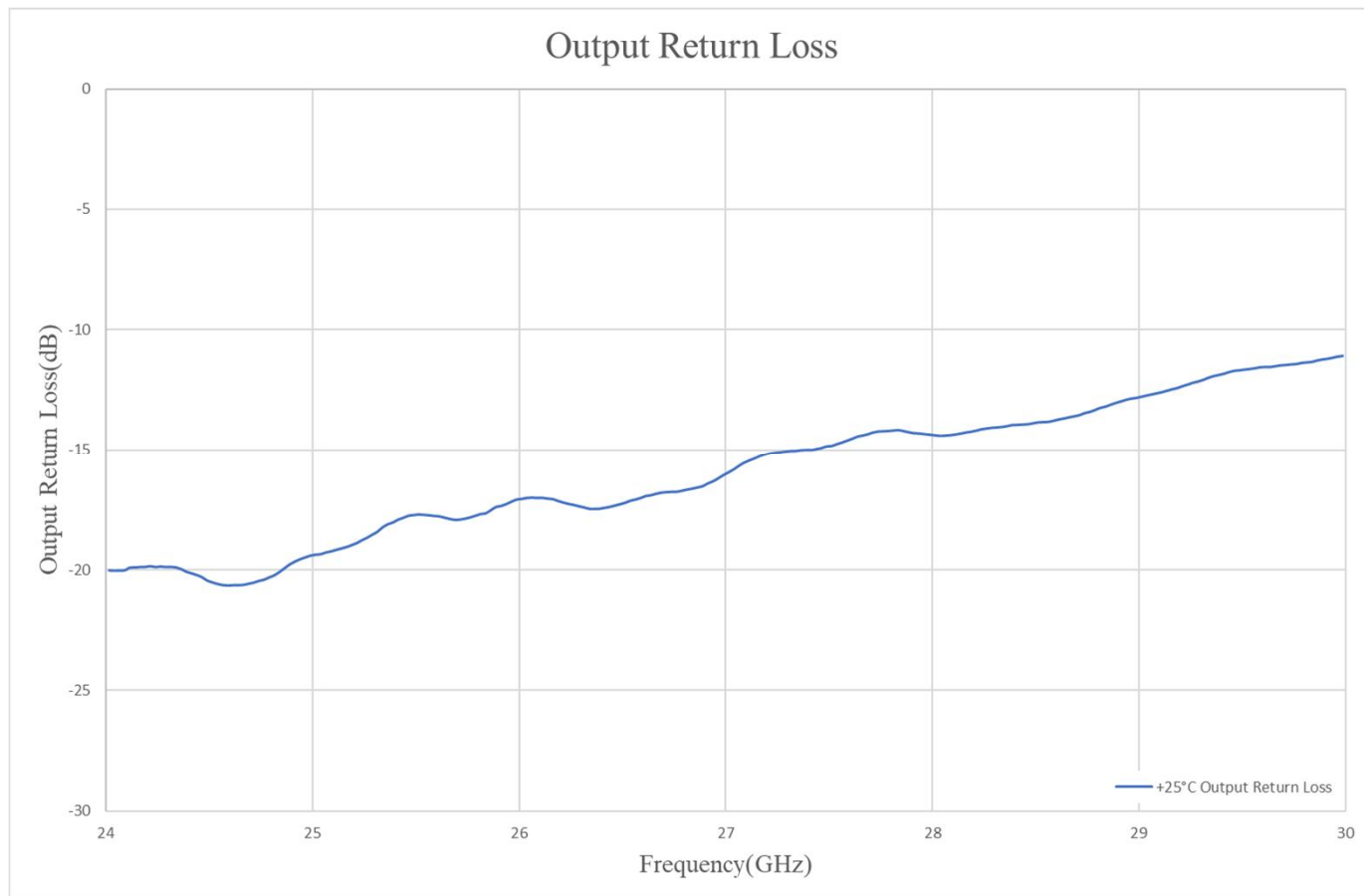


Typical Performance

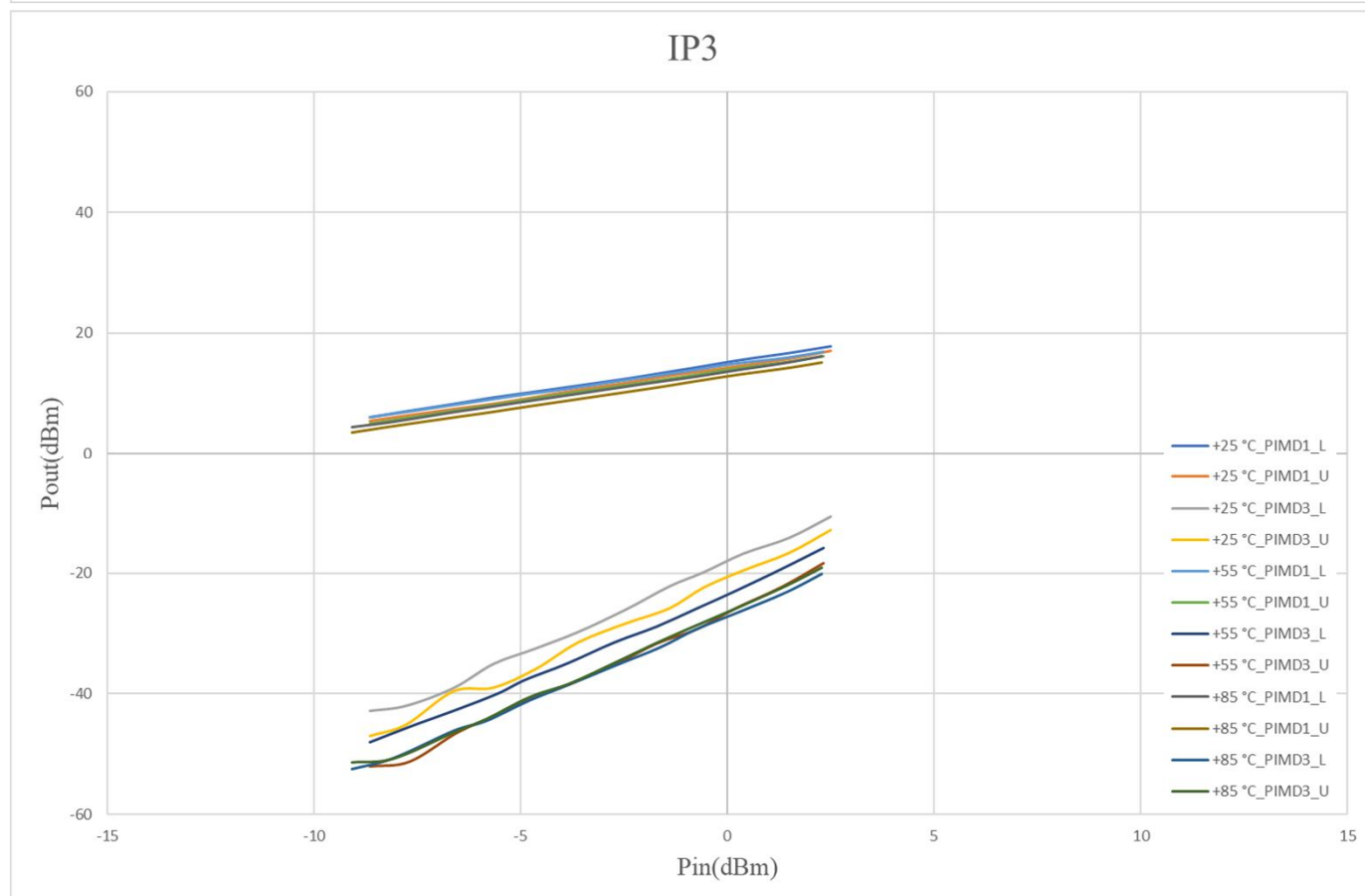
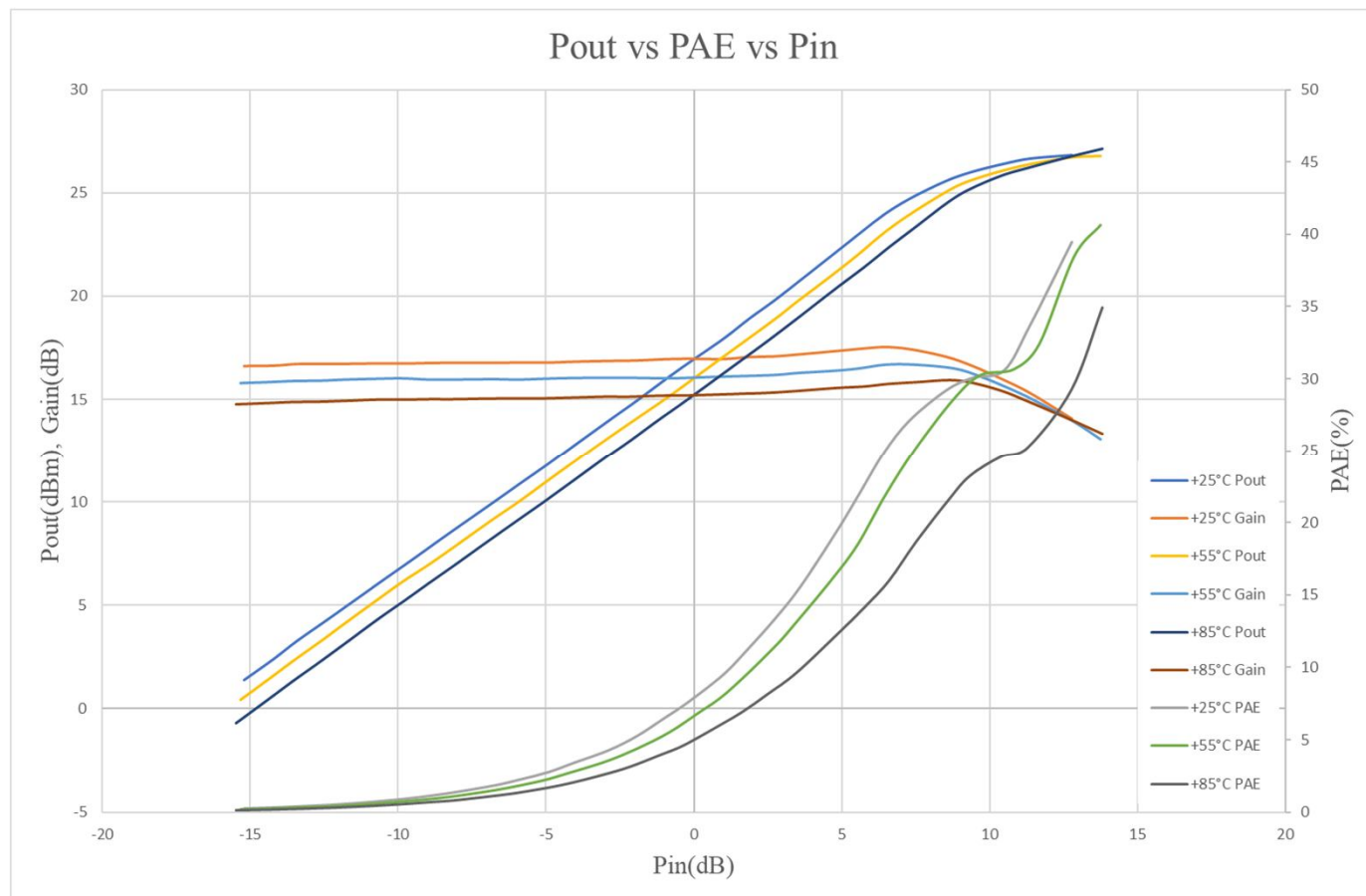




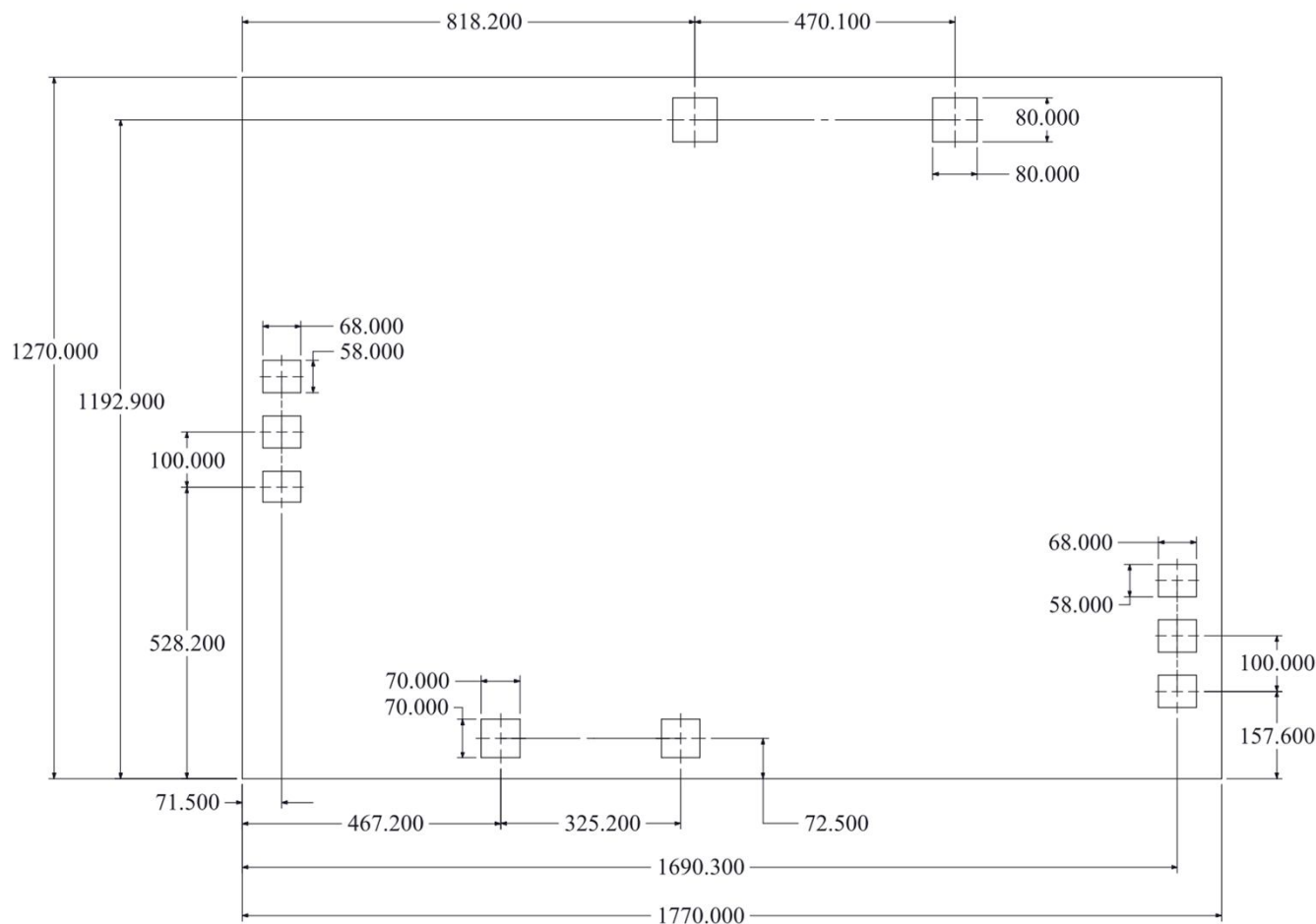
Typical Performance



Typical Performance



Mechanical Information



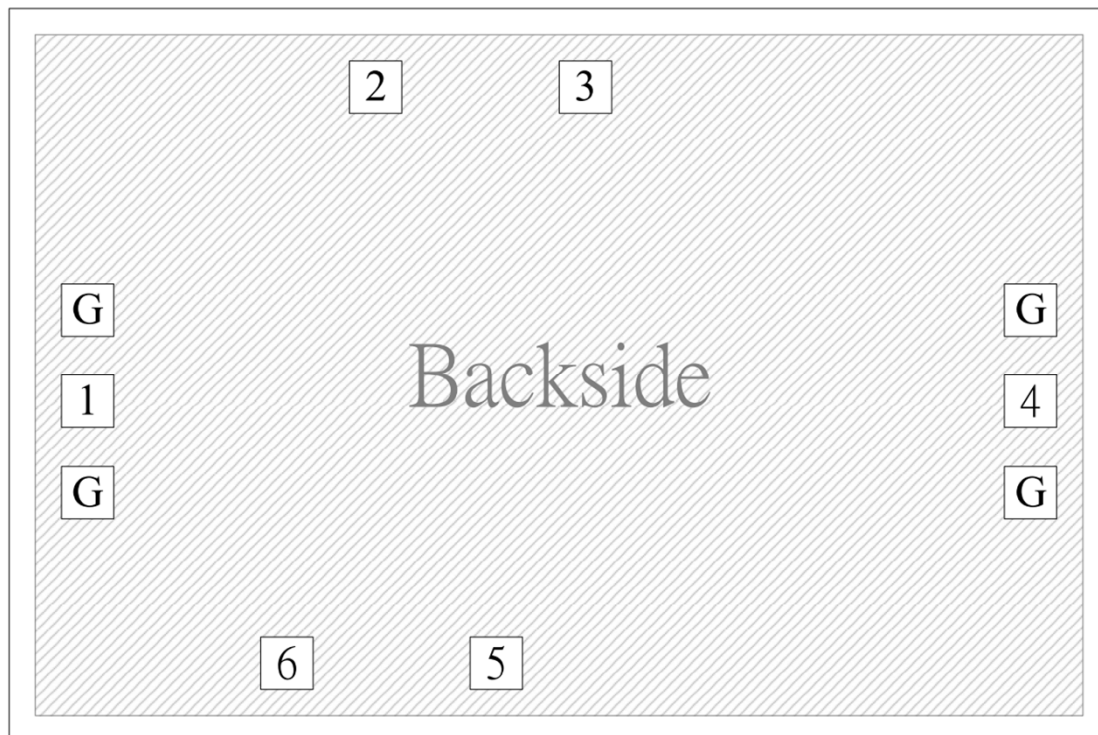
Notes:

1. RF PAD size: 68 μm \times 58 μm
2. GND PAD size: 68 μm \times 58 μm
3. Drain PAD size: 80 μm \times 80 μm
4. Gate PAD size: 70 μm \times 70 μm
5. Die thickness: 100 μm
6. Backside and bond pad metal: Gold
7. Backside is RF and DC ground

Unit: μm

Pad Description

Pinout and Function Description



Pin Function Description

PIN#	Function	Notes
1	RF_IN	This pin is matched to 50 Ω and built-in DC blocks
2	V_{d1}	Drain Voltage
3	V_{d2}	Drain Voltage
4	RF_OUT	This pin is matched to 50 Ω and built-in DC blocks
5	V_{g2}	Gate Voltage
6	V_{g1}	Gate Voltage
G	GND	Connect to RF and DC Ground
Backside	GND	Connect to RF and DC Ground

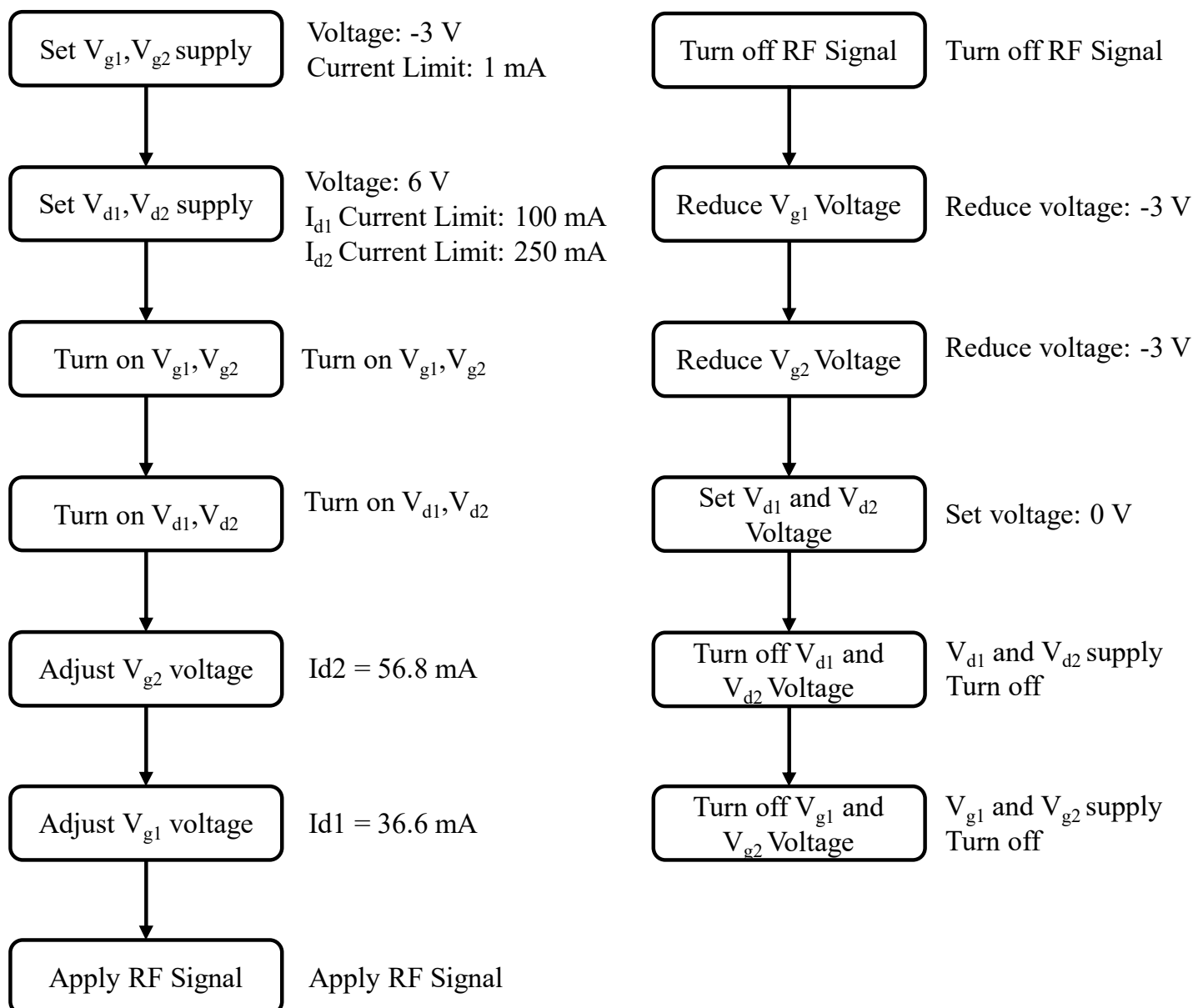
Application Information

Power-up Sequence

- 1) Set V_{g1}, V_{g2} voltage to -3 V, limit current to 1 mA
- 2) Set V_{d1} voltage to 6 V, limit current to 100 mA
- 3) Set V_{d2} voltage to 6 V, limit current to 250 mA
- 4) Turn on V_{g1}, V_{g2} supply
- 5) Turn on V_{d1}, V_{d2} supply
- 6) Adjust V_{g2} more positive until $I_{d2} = 56.8$ mA
- 7) Adjust V_{g1} more positive until $I_{d1} = 36.6$ mA
- 8) Apply RF signal

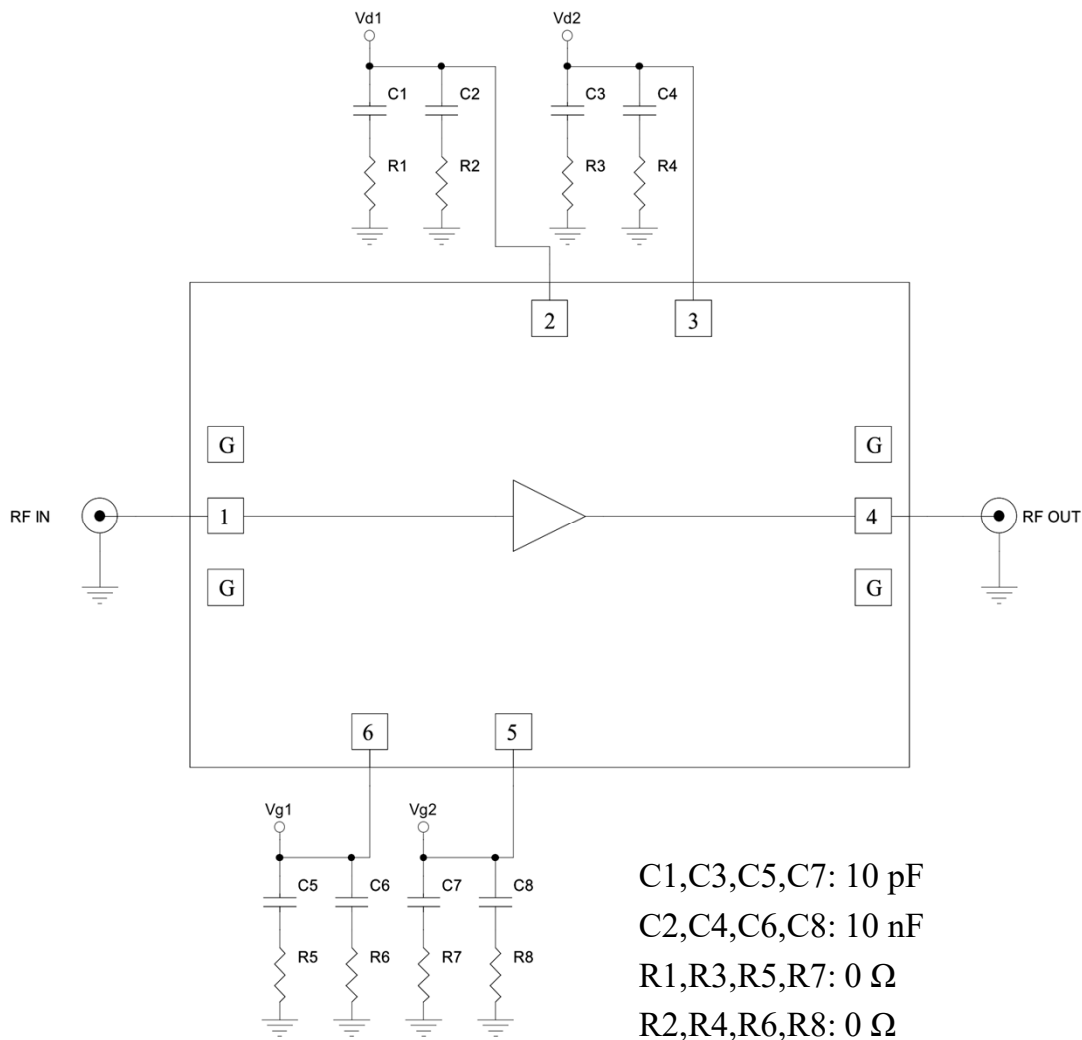
Power-down Sequence

- 1) Turn off RF signal
- 2) Reduce V_{g1} to -3 V, ensure $I_{d1} = 0$ mA
- 3) Reduce V_{g2} to -3 V, ensure $I_{d2} = 0$ mA
- 4) Set V_{d1}, V_{d2} voltage to 0 V
- 5) Turn off V_{d1}, V_{d2} supply
- 6) Turn off V_{g1}, V_{g2} supply



Application Information

Application Schematic



Application Information

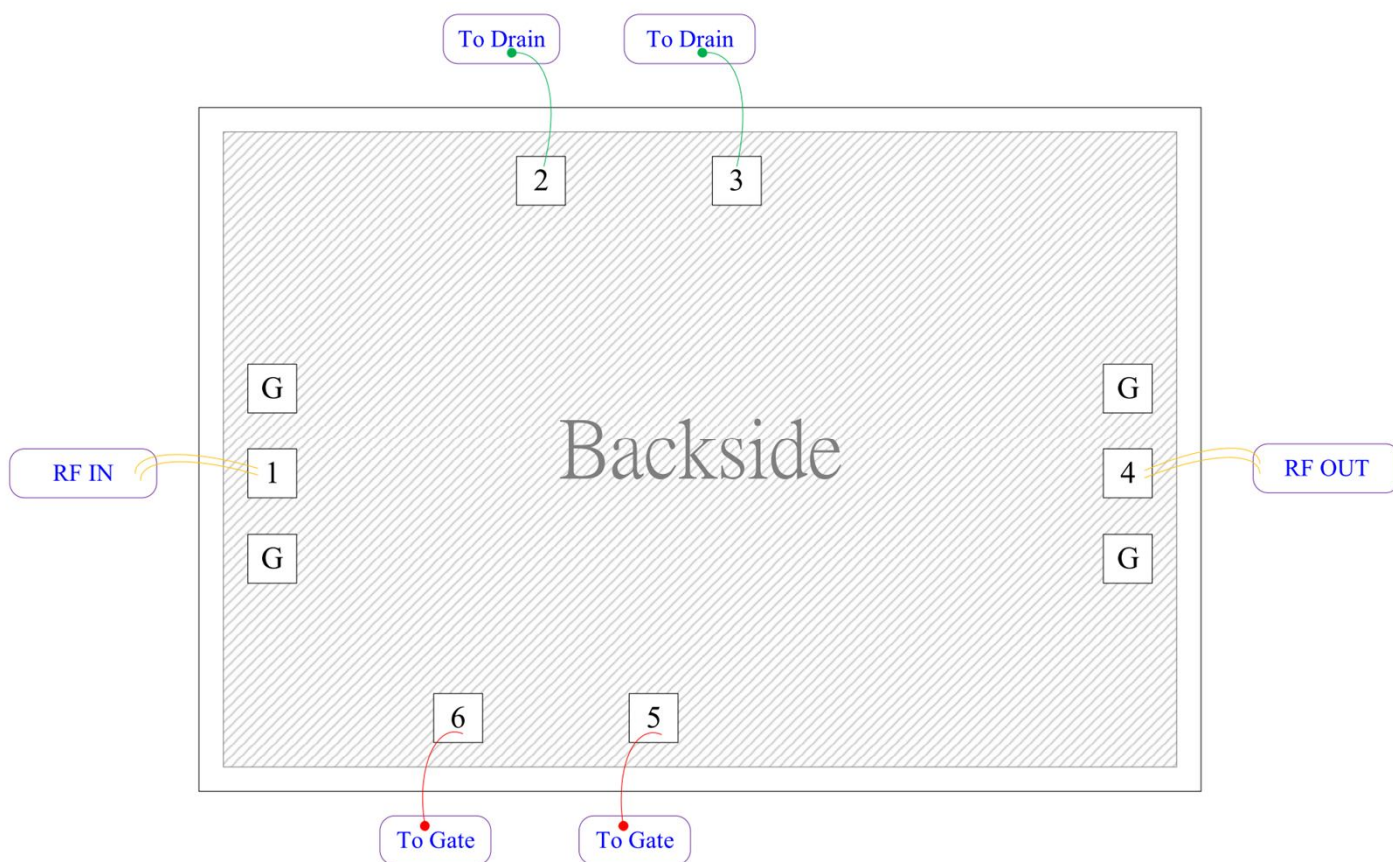
Assembly Guidelines

The URP5A98 backside pad is RF and DC ground, die assembly operations be performed under lamellar flow or in an environment maintained at Class 1000, or better. Die attach should be accomplished with electrically and thermally conductive epoxy only, eutectic attach is not recommended. The top surface of the semiconductor should be made planar to the adjacent RF transmission lines, and the RF decoupling capacitors placed in close proximity to the DC connections on chip.

RF connections should be made as short as possible to reduce the inductive effect of the bond wire.

This chip thickness is 100 μm and should be handled by the sides of the die or with a custom collet. Do not make contact directly with the die surface as this will damage the monolithic circuitry. Handle with care.

Assembly Diagram



Note: GaAs pHEMT dies are susceptible to chipping and cracking if not properly been handled, causing reliability concerns.



Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices

ESD Precaution:

Protection must be afforded for the personnel, equipment, and working environment. Employees handling die must wear static dissipative wrist straps. Both the worktables and floors (or local floor mats) must be grounded to allow for static dissipation as well. Work-in-process and finished goods must be stored in an ESD protected environment. Static induced failures are often latent. The damage may not be obvious at the time of exposure of the die to ESD. Therefore, it is a good practice to insure that both the working environment and the handling techniques are compliant with the requirements for handling devices which are sensitive to ESD.

RoHS Compliance

RoHS:	UltrabandTech defines “RoHS” to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, “RoHS” products are suitable for use in specified lead-free processes. UltrabandTech may reference these types of products as "Pb-Free".
RoHS Exempt:	UltrabandTech defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green:	UltrabandTech defines “Green” to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000 ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000 ppm threshold requirement.

Important Notice

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