URL6C48 mmWave LNA

UltrabandTech

Product Overview

The URL6C48 is a GaN HEMT based with high gain and linearity, low noise MMIC amplifier in die form, the excellent power robust characteristic combining high gain, flatness and low noise figure, making it ideal for high power applications.

Key Features

- 25 to 31 GHz frequency range
- Gain flatness ±0.6 dB from 26.5 to 29.5 GHz
- NF: 2.5 dB @ 28 GHz
- IP_{1dB}: 4 dBm @ 28 GHz
- IIP_3: 16 dBm @ 28 GHz
- Built-in DC Blocks

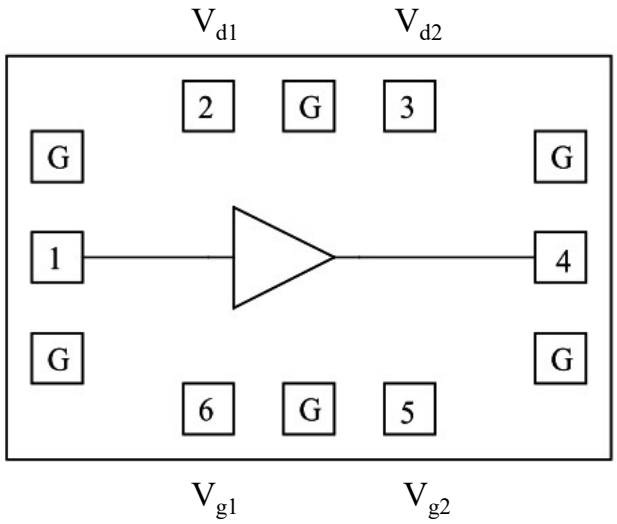
Application

- 5G FR2 Antenna Modules
- FWA
- Satcom
- Radar

Ordering Information

Part Number	Package
URL6C48	Die

Functional Block Diagram



Absolute Maximum Ratings

Parameters	Rating	Unit
DC Drain Voltage	25	V
CW Incident Power	> 6	dBm
Operating Temperature	-40°C to +85°C	°C
Storage Temperature	-65°C to +150°C	°C

Recommended Operating Conditions

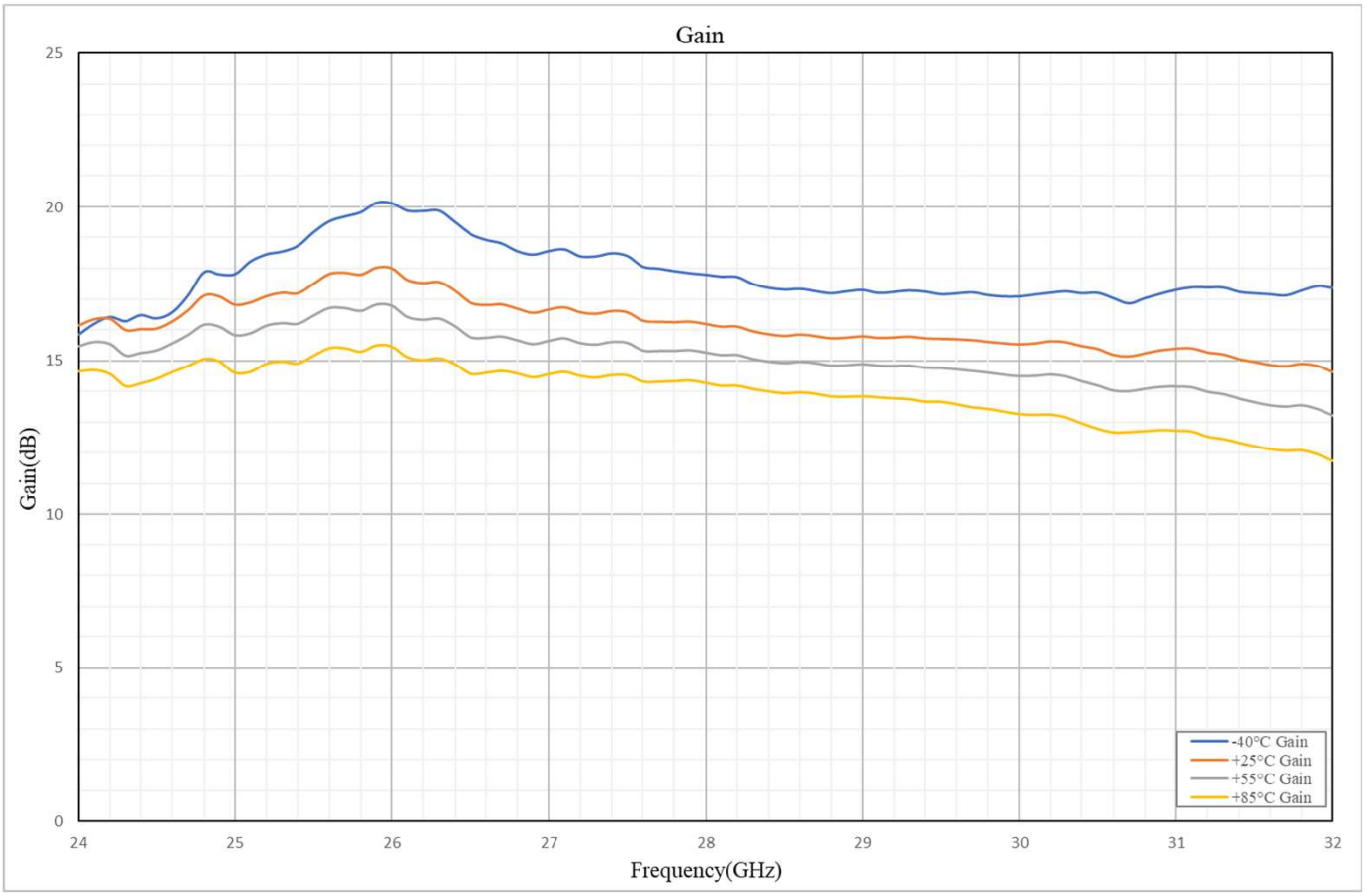
Parameter	Value	Unit
V_{d1}, V_{d2}	10	V
V_{g1}	-1.53	V
I_{d1} (Quiescent)	9.9	mA
V_{g2}	-1.27	V
I_{d2} (Quiescent)	19.9	mA

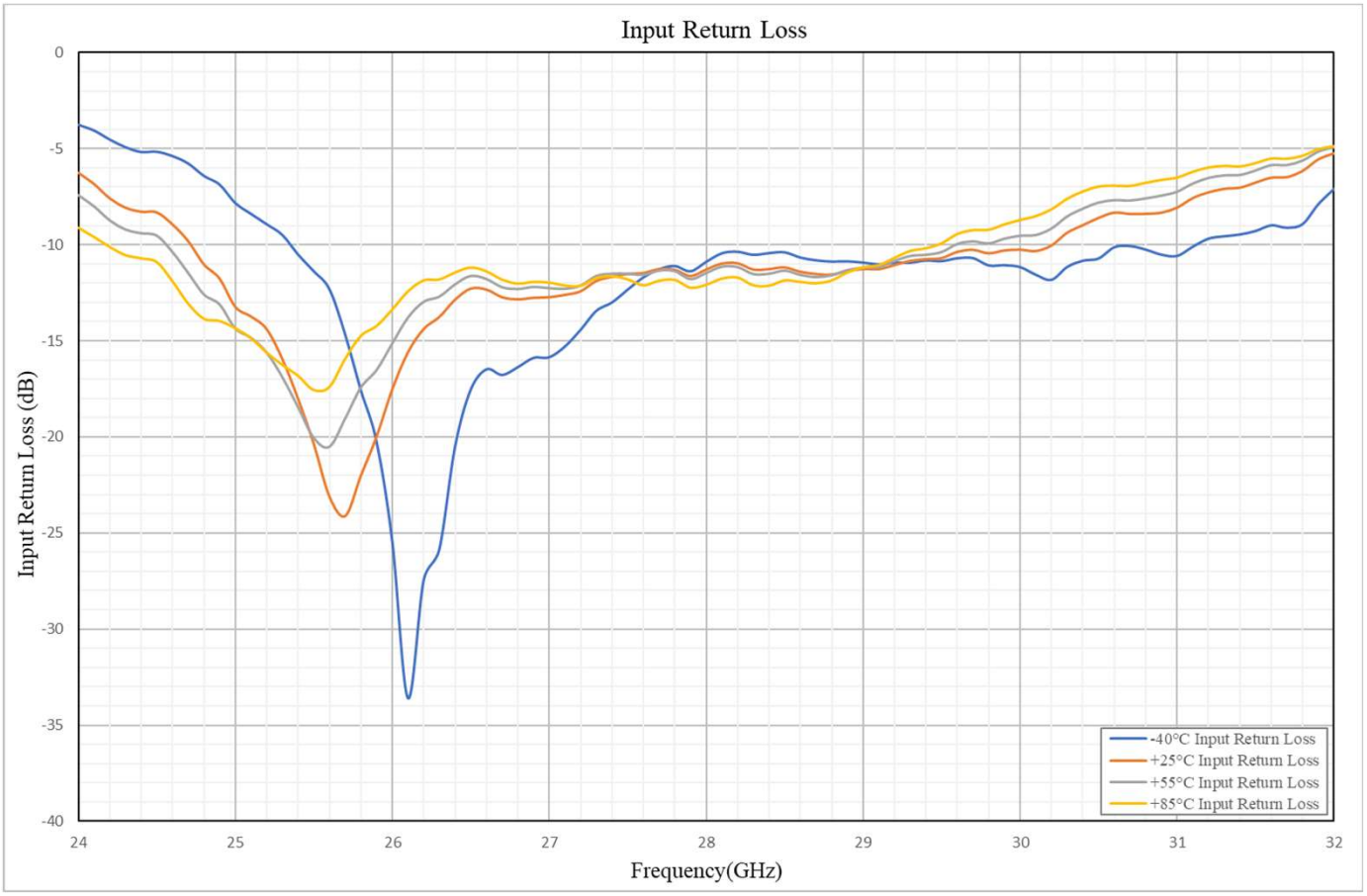
Electrical Specifications (T_A = 25 °C, V_{d1} ,V_{d2}= 10 V, I_{d1} = 9.9 mA , I_{d2} = 19.9 mA, Z_0 = 50 Ω)

Parameters	Min.	Typ.	Max.	Unit
Frequency	25		31	GHz
Linear gain	14.6	15.9		dB
Gain flatness		±1.3		dB
Gain variation over temperature		-0.033		dB / °C
Isolation	34.1	37.3		dB
Noise Figure		2.8	3.5	dB
Input Return Loss	7.4	11.8		dB
Output Return Loss	6.1	15.0		dB
Input P_{1dB} @ 28 GHz		4		dBm
Input IP_3 @ 28 GHz (1)		16(2)		dBm

Note:
(1) 2 tone testing with 10 MHz spacing
(2) -5 dBm input power applied

Typical Performance





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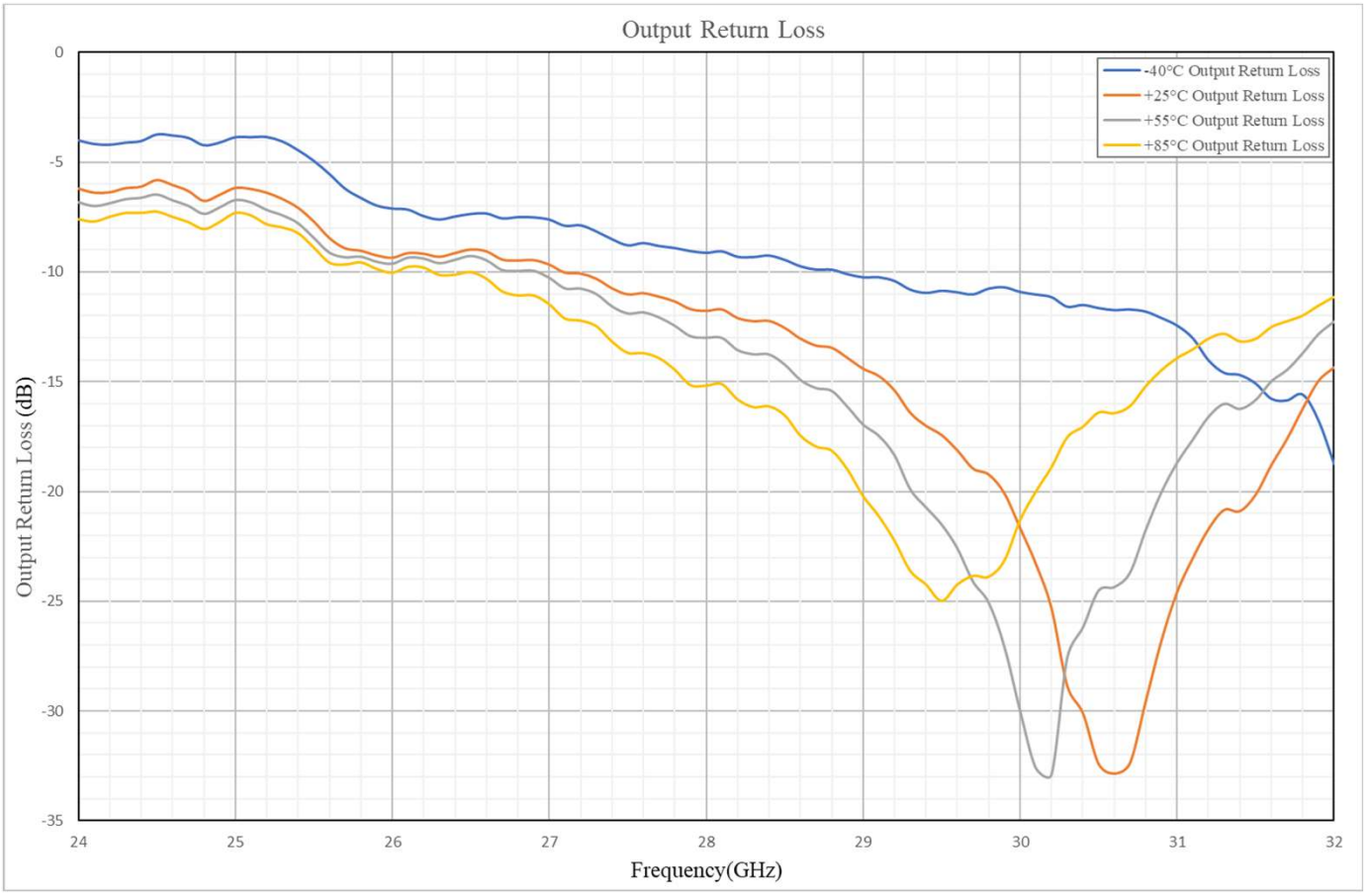
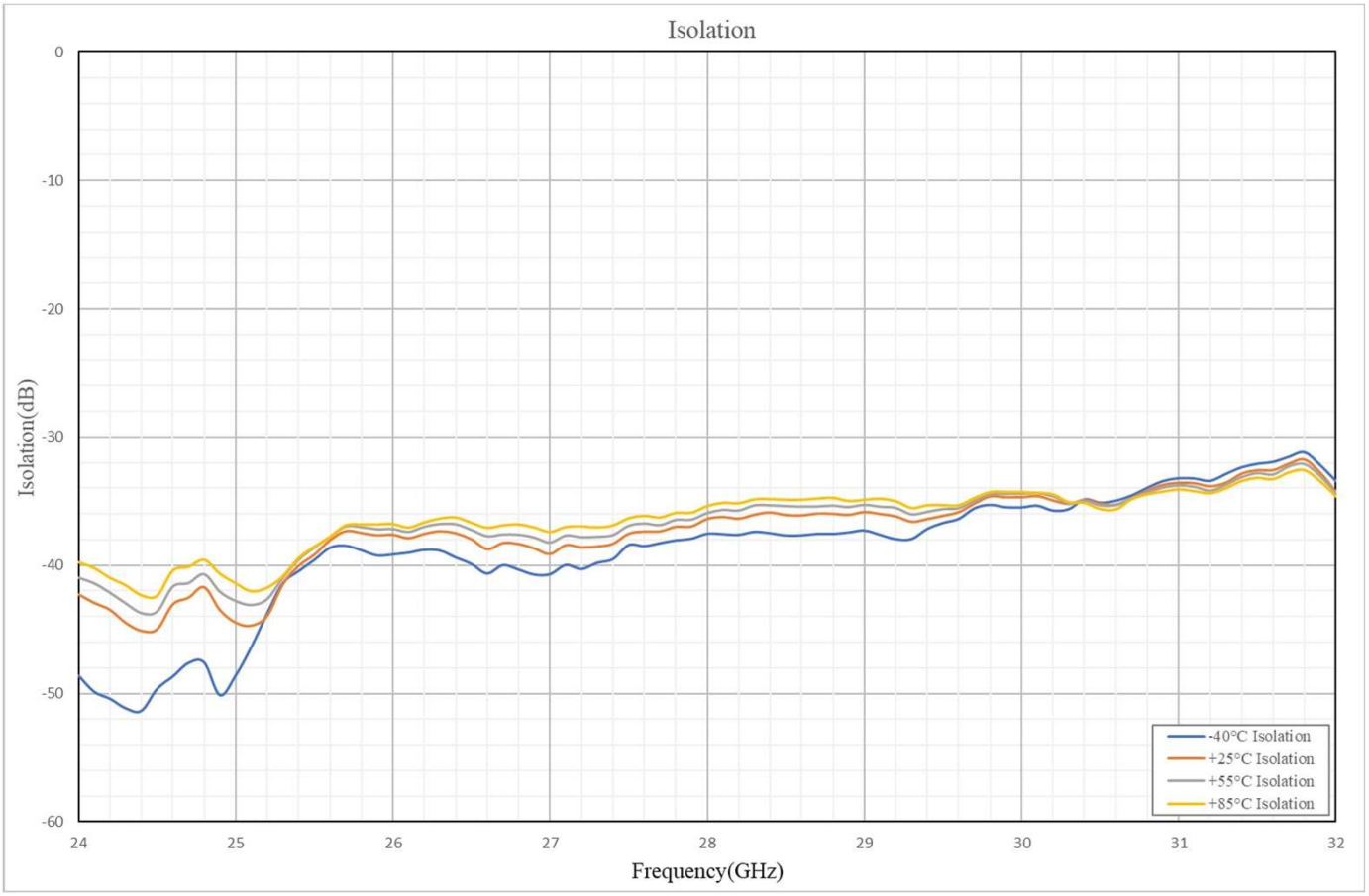
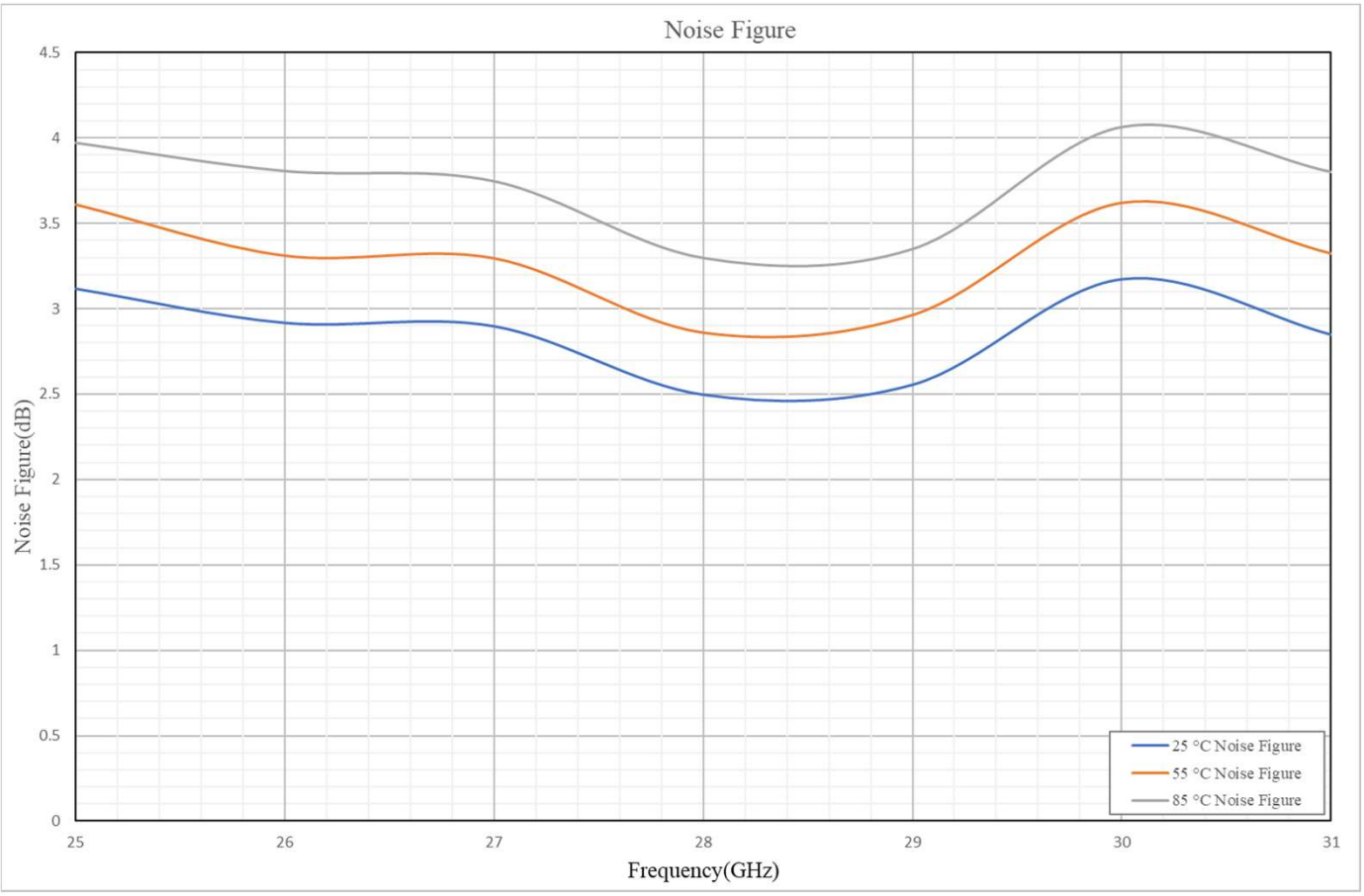
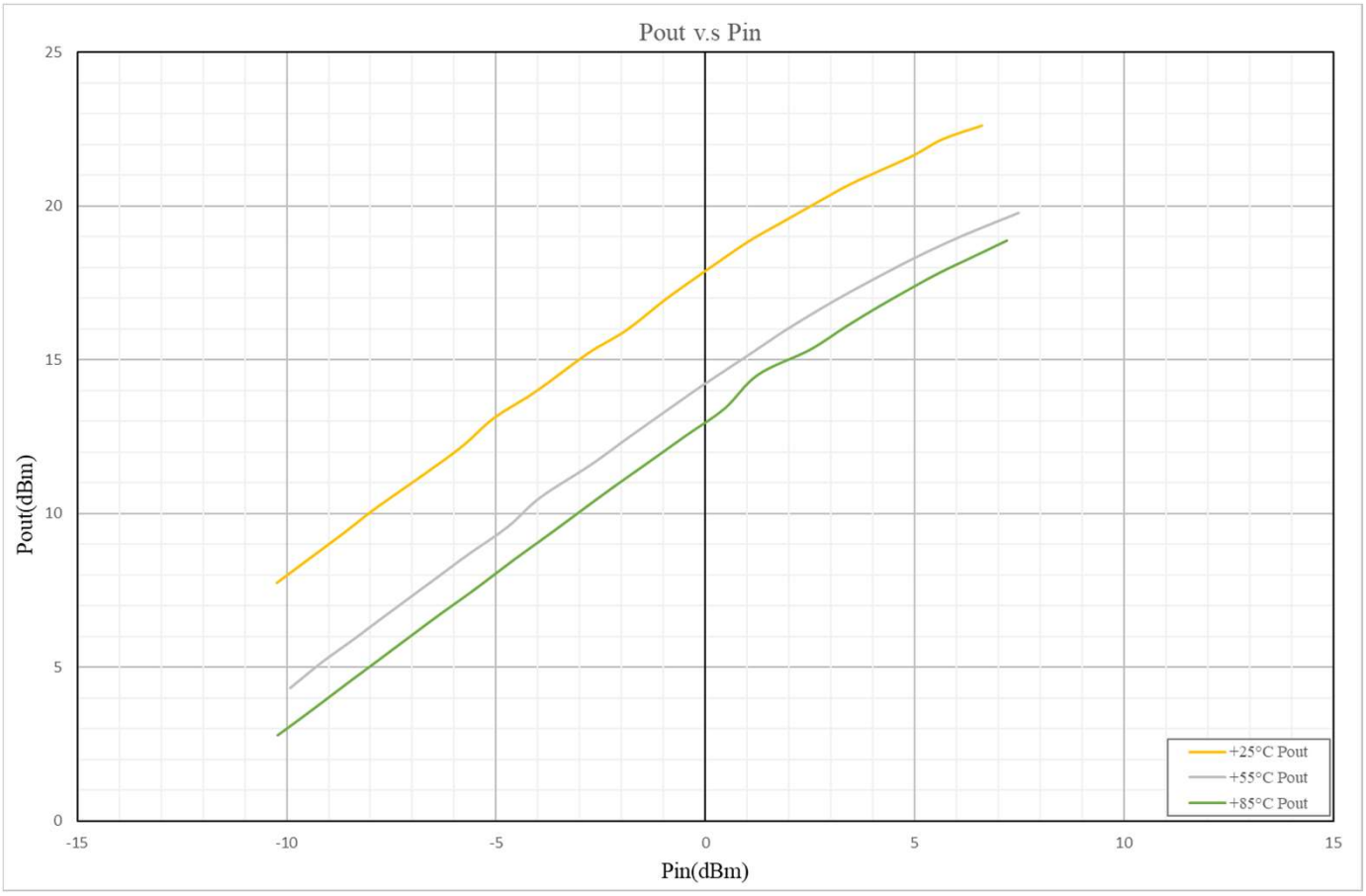


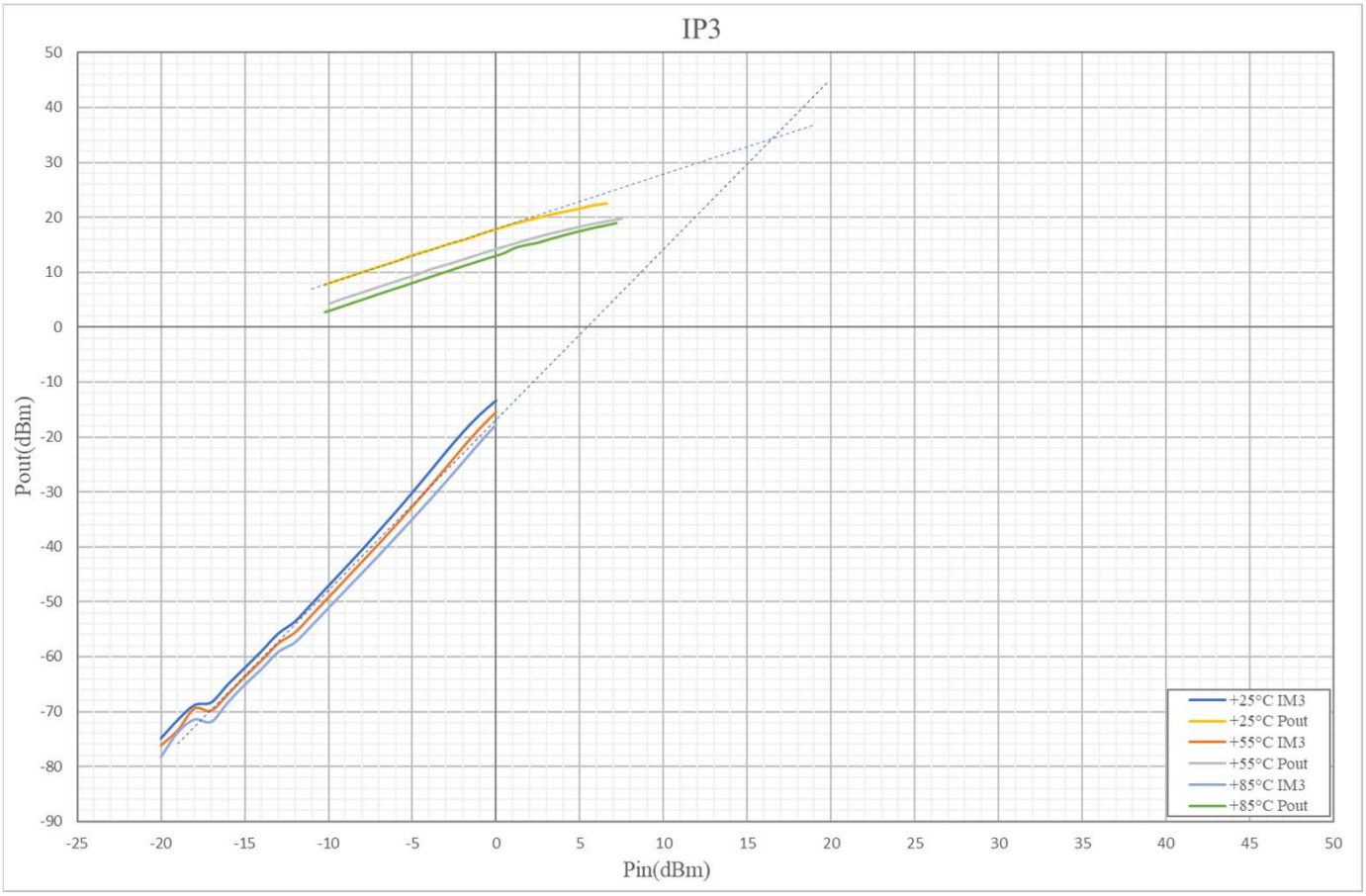


Typical Performance

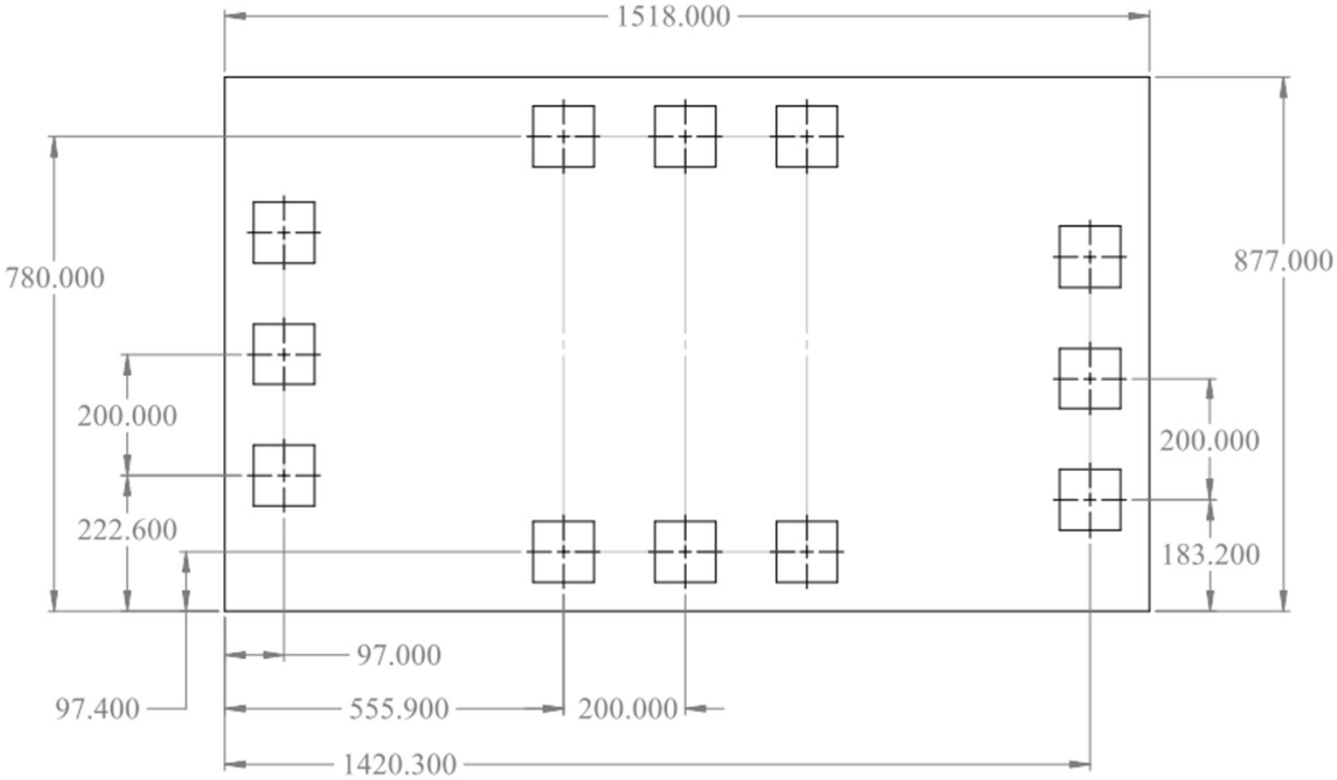


Typical Performance





Mechanical Information

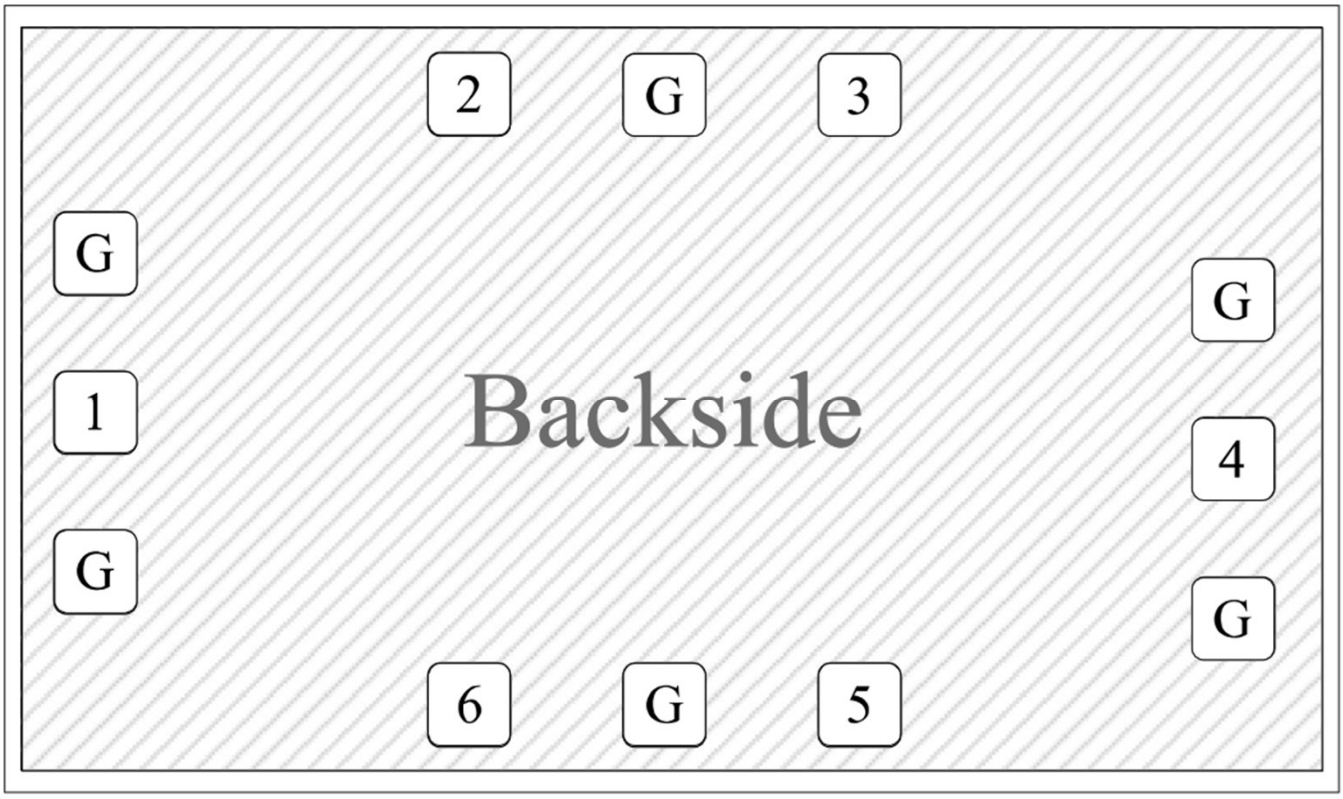


Unit: μm

Note:
1. PAD size: 100 μm × 100 μm
2. Die thickness: 100 μm
3. Backside and bond pad metal: Gold
4. Backside is RF and DC ground

Pad Description

Pinout and Function Description



Pin Function Description

PIN#	Function	Notes
1	RF_IN	This pin is matched to 50 Ω and built-in DC blocks
2	V_{d1}	Drain Voltage
3	V_{d2}	Drain Voltage
4	RF_OUT	This pin is matched to 50 Ω and built-in DC blocks
5	V_{g2}	Gate Voltage
6	V_{g1}	Gate Voltage
G	GND	Connect to RF and DC Ground
Backside	GND	Connect to RF and DC Ground

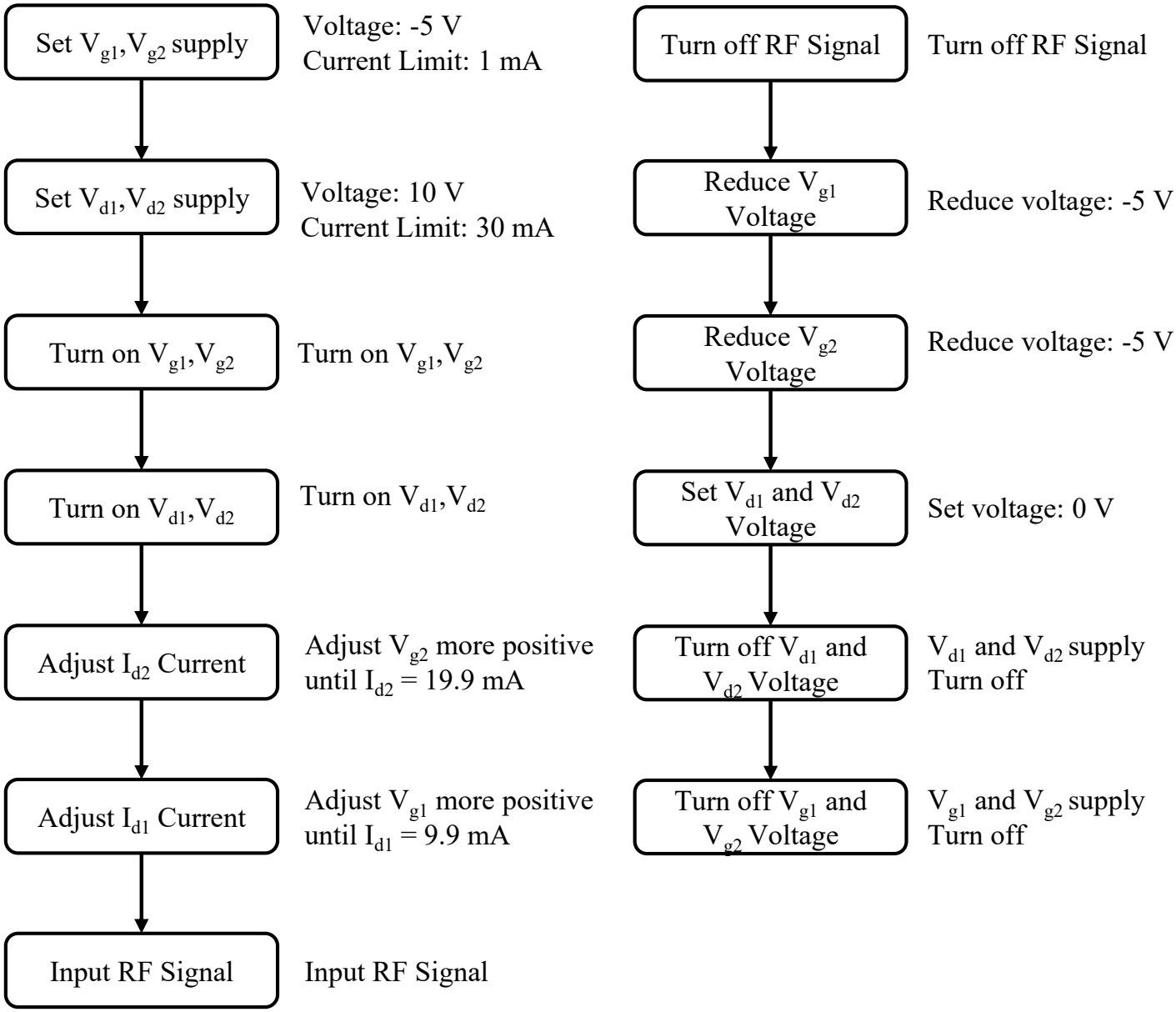
Application Information

Power-up Sequence

1) Set V_{g1},V_{g2} voltage to -5 V, limit current to 1 mA
2) Set V_{d1},V_{d2} voltage to 10 V, limit current to 30 mA
3) Turn on V_{g1},V_{g2} supply
4) Turn on V_{d1},V_{d2} supply
5) Adjust V_{g2} more positive until I_{d2} = 19.9 mA
6) Adjust V_{g1} more positive until I_{d1} = 9.9 mA
7) Apply RF signal

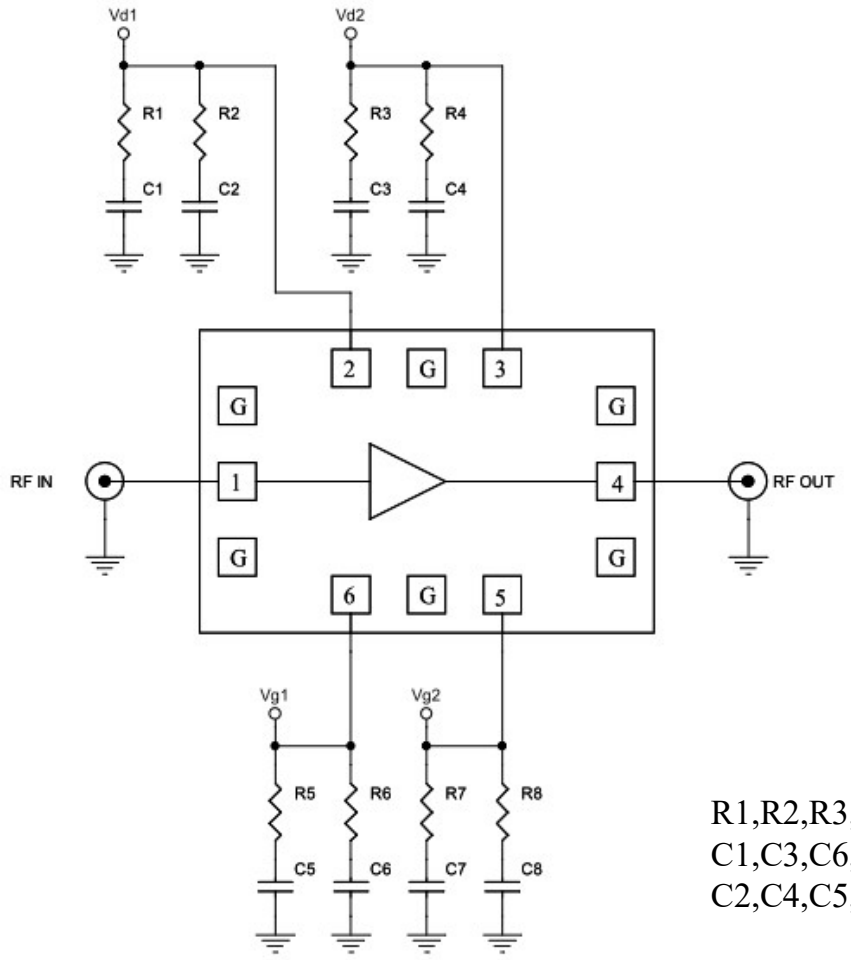
Power-down Sequence

1) Turn off RF signal
2) Reduce V_{g1} to -5 V, ensure I_{d1} = 0 mA
3) Reduce V_{g2} to -5 V, ensure I_{d2} = 0 mA
4) Set V_{d1},V_{d2} voltage to 0 V
5) Turn off V_{d1},V_{d2} supply
6) Turn off V_{g1},V_{g2} supply



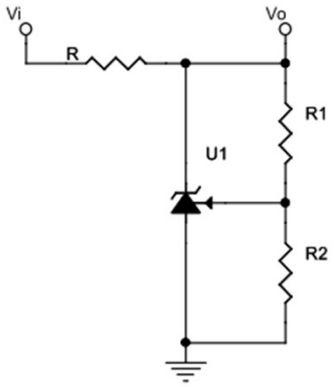
Application Information

Application Schematic



R1,R2,R3,R4,R5,R6,R7,R8: 0Ω
C1,C3,C6,C8: 10 pF
C2,C4,C5,C7: 10 nF

Drain Voltage Conversion Schematic



R: 10 Ω
R1: 10K Ω
R2: 3.3K Ω
U1: TL431

Note:
1. Drain voltage can be generated using a resistor divider or using TL431
2. R1 and R2 resistor use 1% or higher precision

Application Information

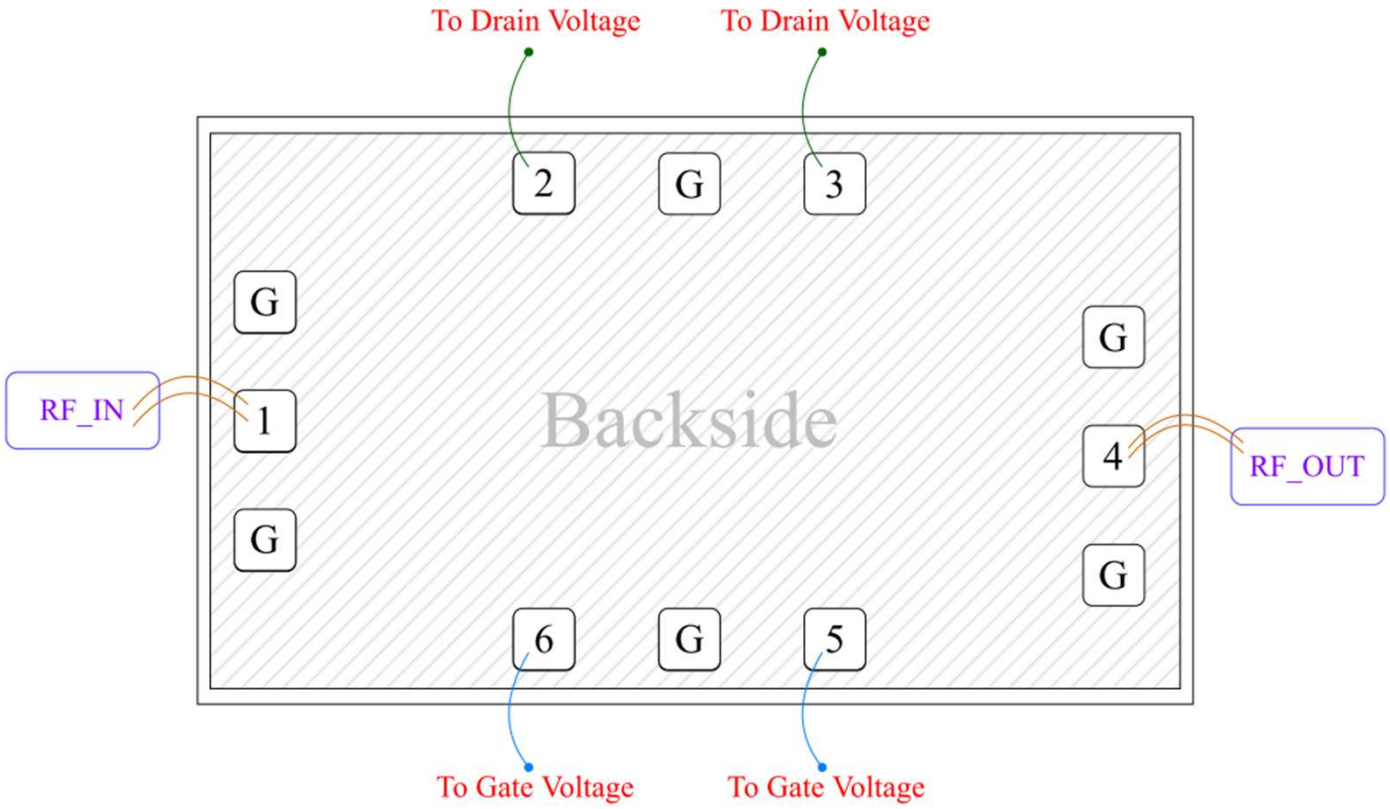
Assembly Guidelines

The URL6C48 backside pad is RF and DC ground, die assembly operations be performed under lamellar flow or in an environment maintained at Class 1000, or better. Die attach should be accomplished with electrically and thermally conductive epoxy only, eutectic attach is not recommended. The top surface of the semiconductor should be made planar to the adjacent RF transmission lines, and the RF decoupling capacitors placed in close proximity to the DC connections on chip.

RF connections should be made as short as possible to reduce the inductive effect of the bond wire.

This chip thickness is 100 µm and should be handled by the sides of the die or with a custom collet. Do not make contact directly with the die surface as this will damage the monolithic circuitry. Handle with care.

Assembly Diagram



Note:
GaN HEMT dies are susceptible to chipping and cracking if not properly been handled, causing reliability concerns.

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices.

ESD Precaution:

Protection must be afforded for the personnel, equipment, and working environment. Employees handling die must wear static dissipative wrist straps. Both the worktables and floors (or local floor mats) must be grounded to allow for static dissipation as well. Work-in-process and finished goods must be stored in an ESD protected environment. Static induced failures are often latent. The damage may not be obvious at the time of exposure of the die to ESD. Therefore, it is a good practice to insure that both the working environment and the handling techniques are compliant with the requirements for handling devices which are sensitive to ESD.

RoHS Compliance

RoHS:	UltrabandTech defines “RoHS” to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, “RoHS” products are suitable for use in specified lead-free processes. UltrabandTech may reference these types of products as "Pb-Free".
RoHS Exempt:	UltrabandTech defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green:	UltrabandTech defines “Green” to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000 ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000 ppm threshold requirement.

Important Notice

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