

# URF6C55

## mmWave Switch LNA Module



UltrabandTech

### Product overview

The URF6C55 is a MMIC integrated the mmWave Switch and LNA in one die, The design by using 0.15  $\mu\text{m}$  GaAs pHEMT devices in a compact die size with excellent performance.

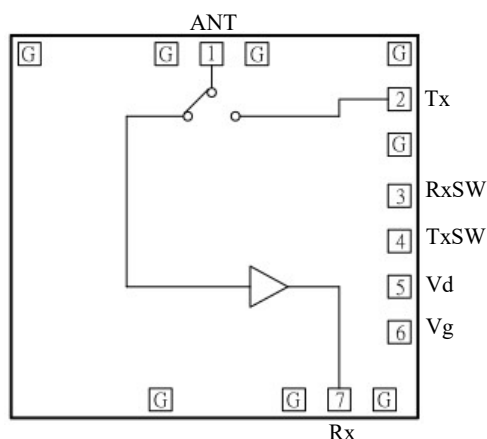
### Key Features

- 25 – 31 GHz frequency range
- MMIC Integrated Switch and LNA
- Fast Switching speed
- Compact size
- Die size 1920  $\mu\text{m}$   $\times$  1758  $\mu\text{m}$

### Application

- 5G FR2 Antenna Modules
- Point-to-Point Wireless
- Satcom

### Functional Block Diagram



### Ordering Information

Part Number	Package
URF6C55	Die

### Truth Table

RF Path	Vbias	
	RxSW	TxSW
ANT to Rx	On	Off
Tx to ANT	Off	On

(1) On: 4 ~ 6 V, Off: 0 V

### Absolute Maximum Ratings

Parameters	Absolute Maximum	Unit
DC Bias Voltage	7	V
CW Incident Power	Ant: 0 dBm Tx: > 26 dBm	dBm
Operating Temperature	-40 °C to +85 °C	°C
Storage Temperature	-65 °C to +150 °C	°C



**Electrical Specifications Rx** ( $T_A = 25\text{ }^\circ\text{C}$ ,  $R_{xSW}/T_{xSW} = 5\text{ V} / 0\text{ V}$ ,  $V_d = 5\text{ V}$ ,  $I_d = 21.5\text{ mA}$ ,  $Z_0 = 50\text{ }\Omega$ )

Parameters	Min.	Typ.	Max.	Unit
Frequency	25		31	GHz
Linear gain	14.5	17.3		dB
Gain flatness(25~29 GHz)		$\pm 1.0$		dB
Gain flatness(29~31 GHz)		$\pm 1.3$		dB
Gain variation over temperature		-0.013		dB / $^\circ\text{C}$
Isolation(Rx-Ant) <sup>(1)</sup>	29.2	31.2		dB
Isolation(Ant-Tx)	17.7	22.7		dB
Noise Figure		4.7	5.8	dB
Input Return Loss	7.6	11.6		dB
Output Return Loss	8.4	13.5		dB
Output $P_{1dB}$ @28 GHz		10		dBm
Output $IP_3$ @28 GHz <sup>(2)</sup>		23.6@-20 dBm		dBm

Note:

1). LNA  $V_g = -0.35\text{V}$

2). 2 tone 10 MHz spacing



**Electrical Specifications Tx** ( $T_A = 25^\circ\text{C}$ ,  $R_{xSW}/T_{xSW} = 0\text{V} / 5\text{V}$ ,  $V_d = 5\text{V}$ ,  $V_g = -2\text{V}$ ,  $Z_0 = 50\Omega$ )

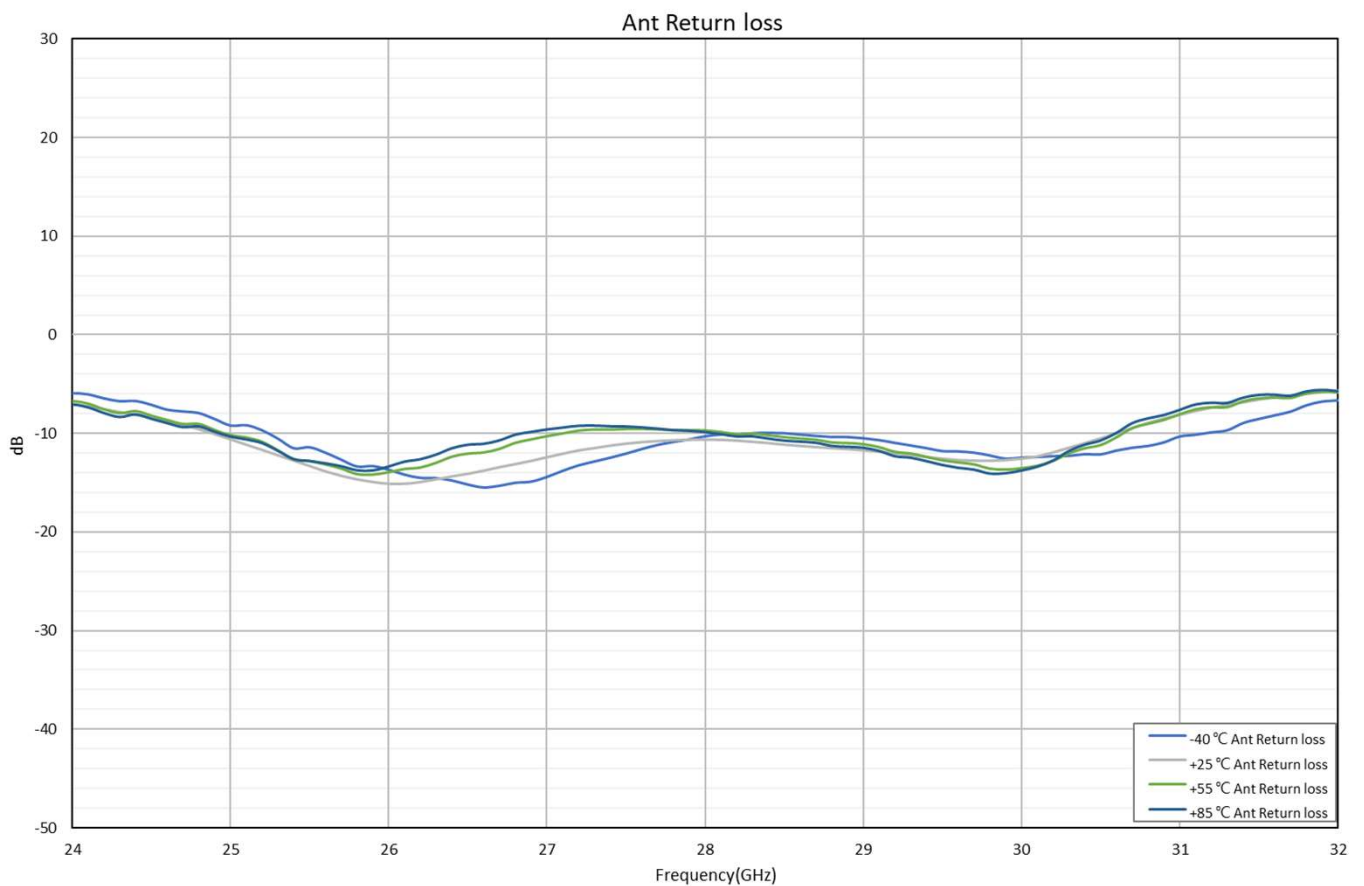
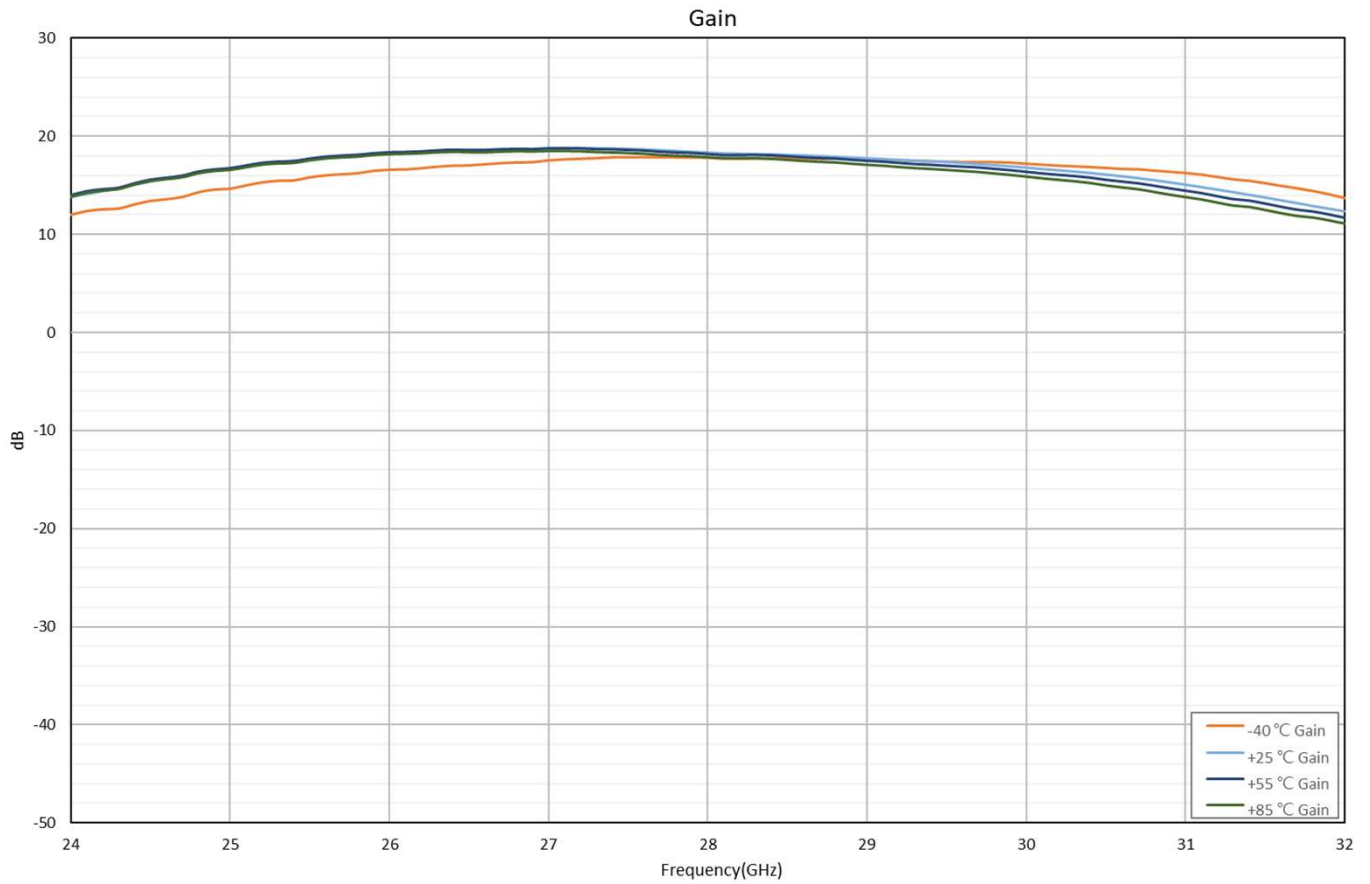
Parameters	Min.	Typ.	Max.	Unit
Frequency	25		31	GHz
Insertion Loss		1.2	1.4	dB
Isolation(Ant-Rx)	41.3	45.3		dB
Isolation(Tx-Rx)	41.7	45.7		dB
Tx Return Loss ON	14.9	24.5		dB
Ant Return Loss ON	11.9	18.6		dB
Input $P_{0.1dB}$		22		dBm
Input $IP_3@28\text{ GHz}^{(3)}$		48.2@10 dBm		dBm
Rise Time - $T_{RISE}$		25 <sup>(1)</sup>		ns
Fall Time - $T_{FALL}$		25 <sup>(2)</sup>		ns

Note:

- 1). Rise Time -  $T_{RISE}$  at 10% to 90% RF
- 2). Fall Time -  $T_{FALL}$  at 90% to 10% RF
- 3). 2 tone 10 MHz spacing

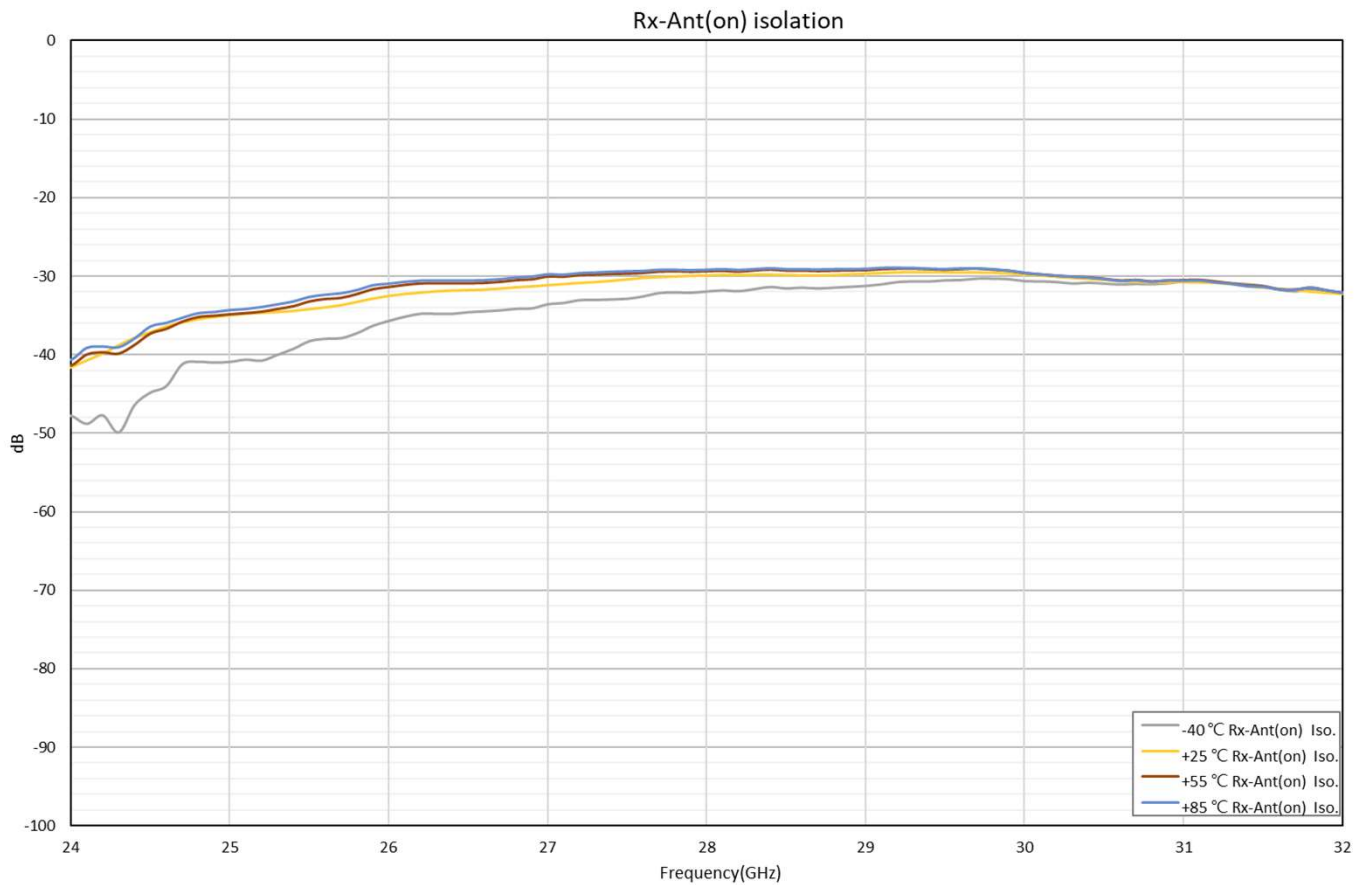
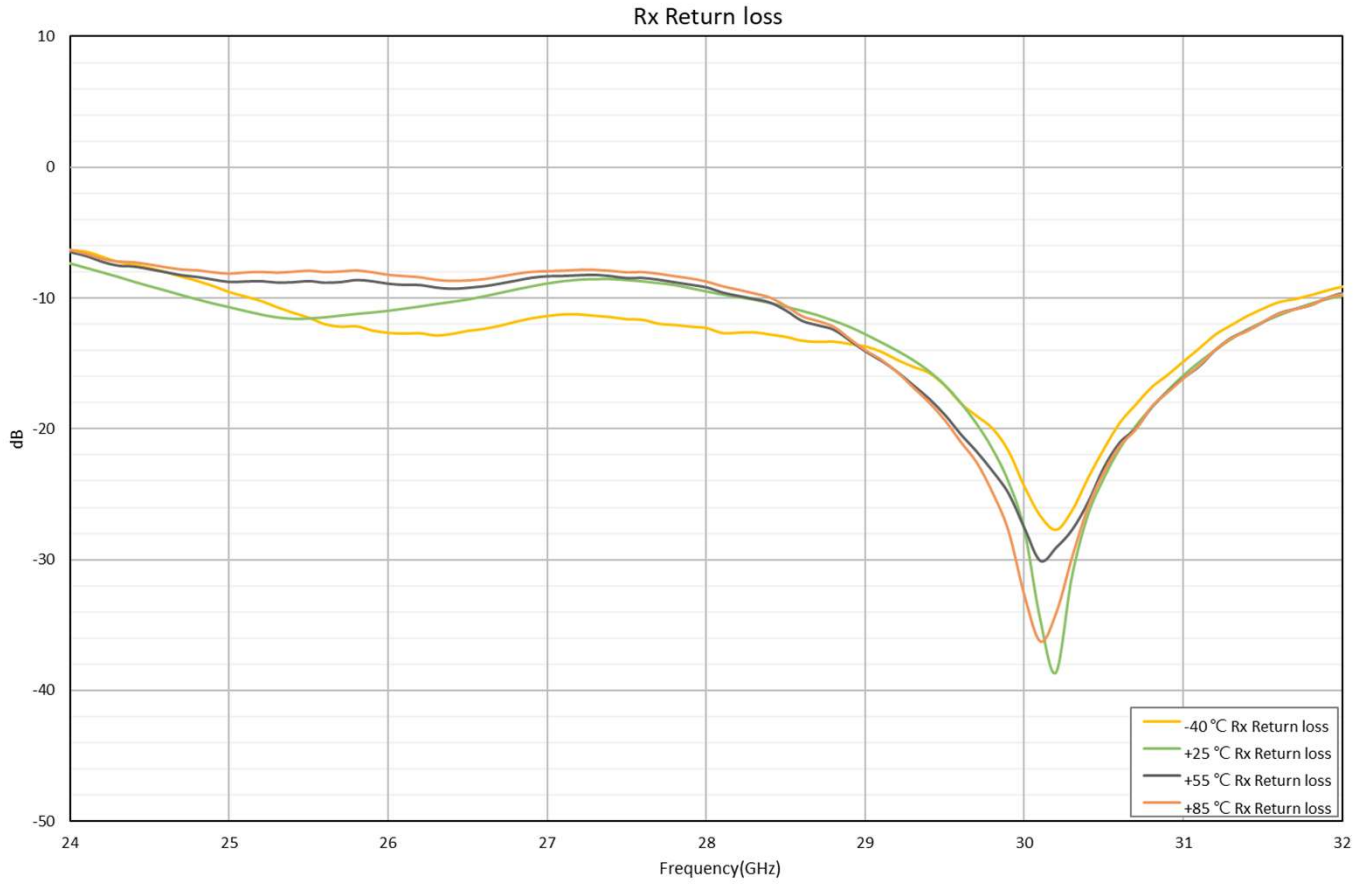


# Typical Performance Rx





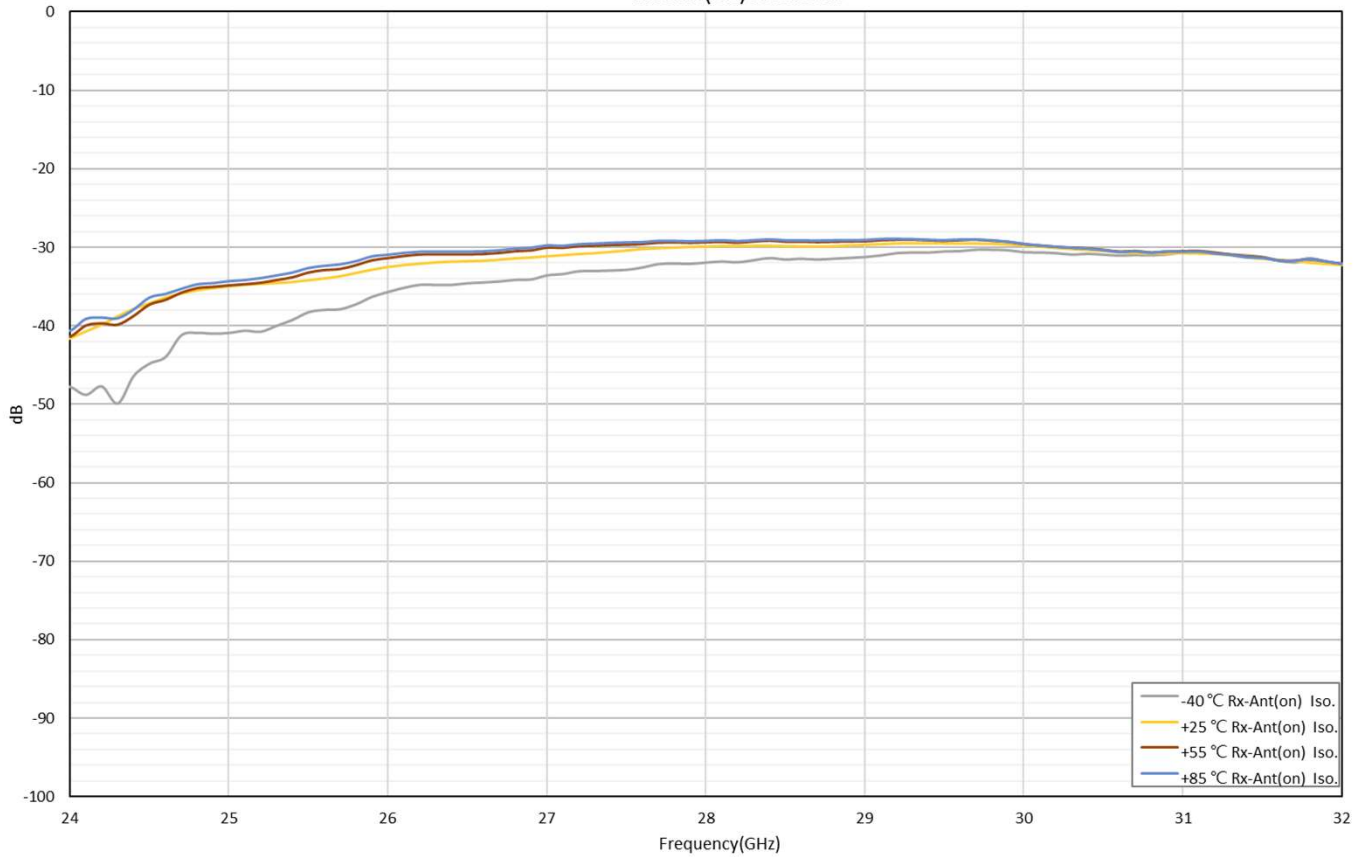
# Typical Performance Rx



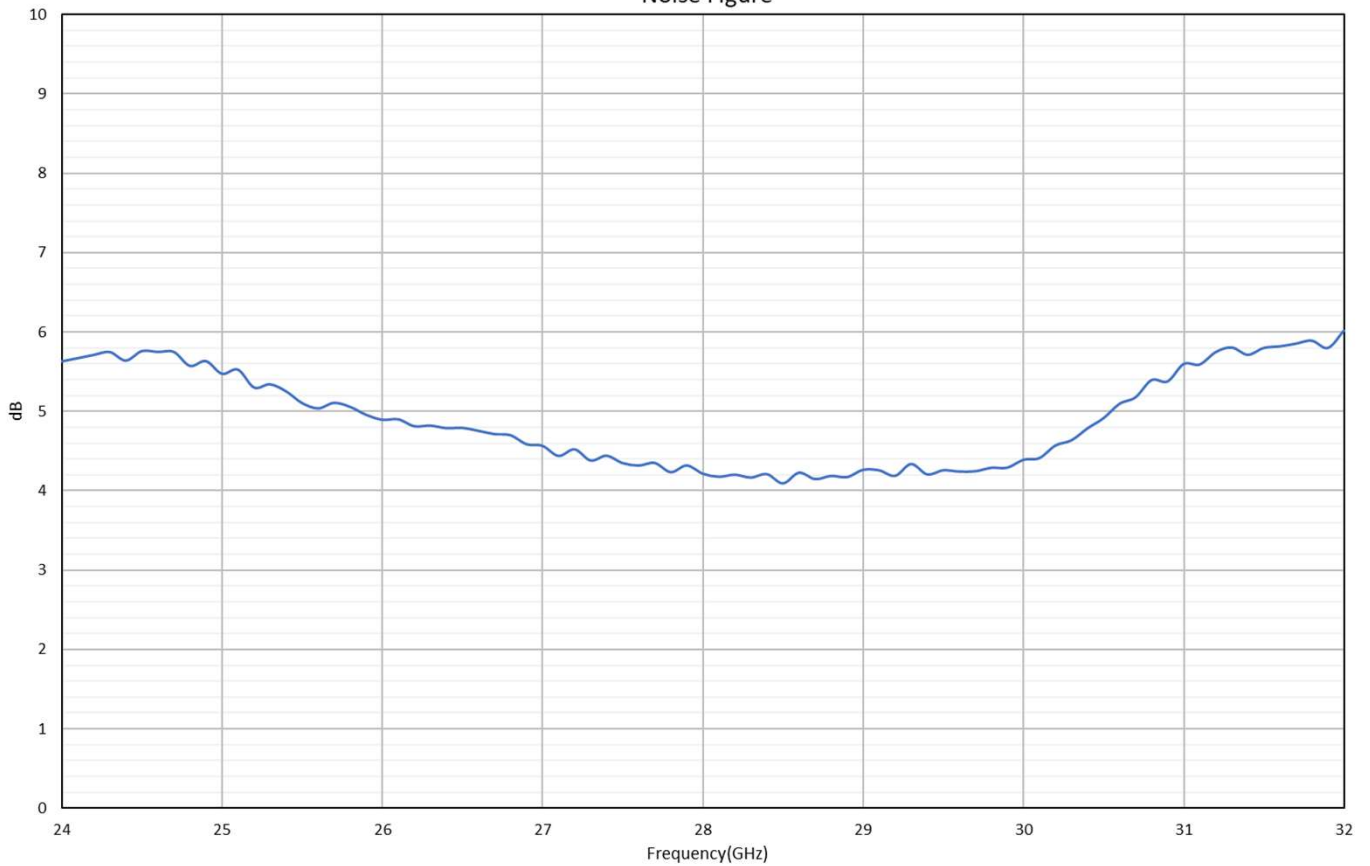


# Typical Performance Rx

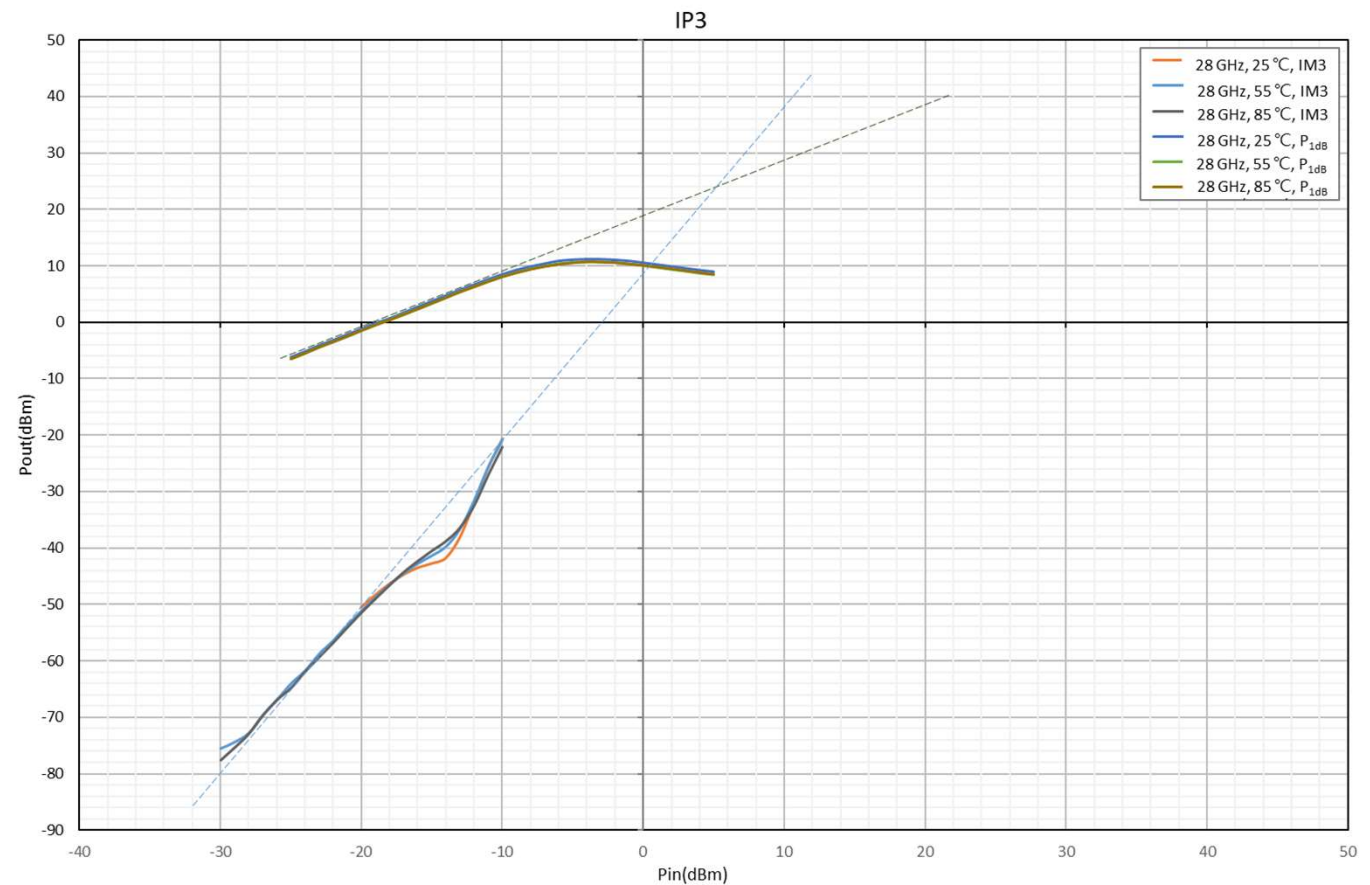
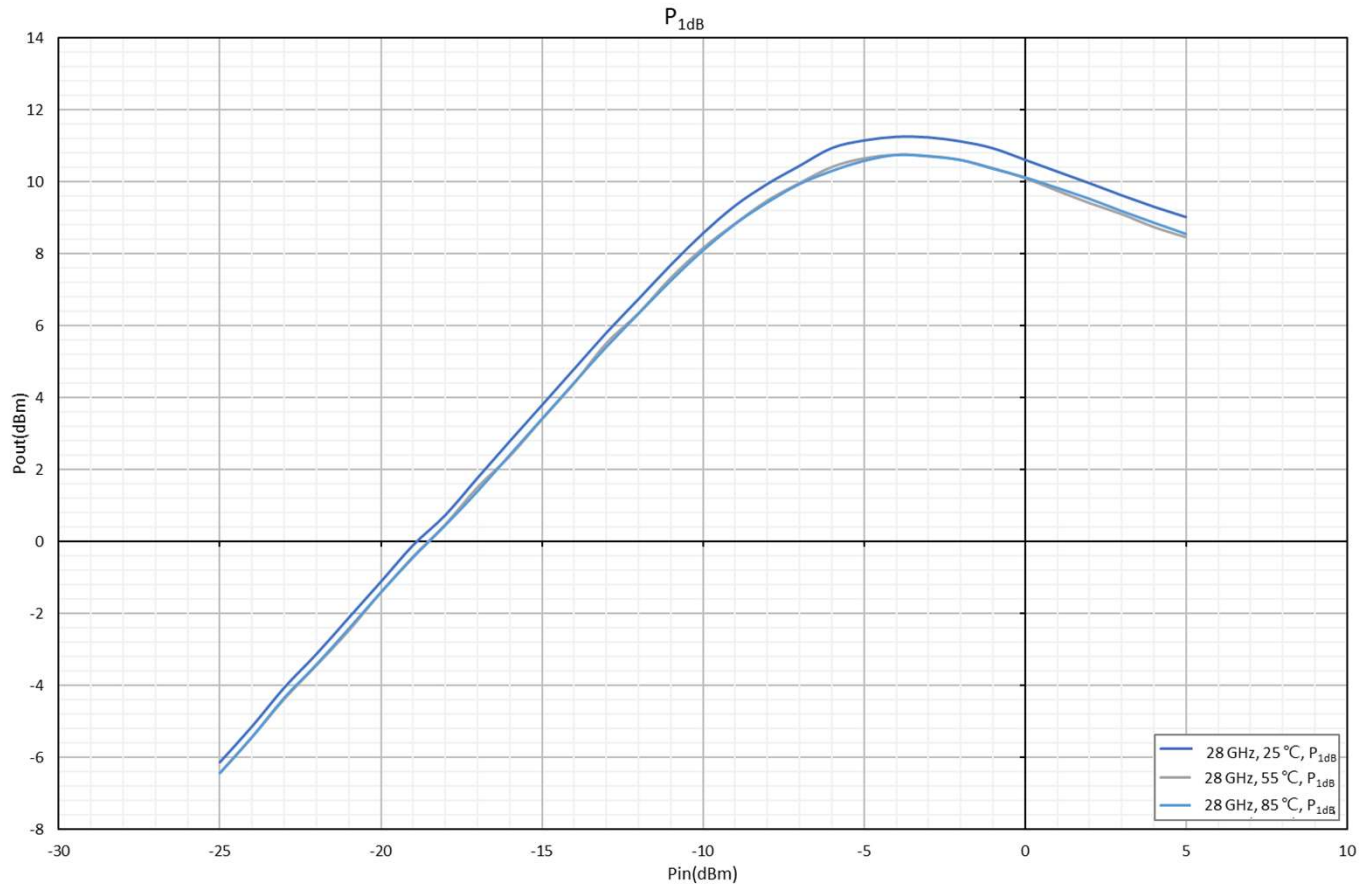
Rx-Ant(on) isolation



Noise Figure

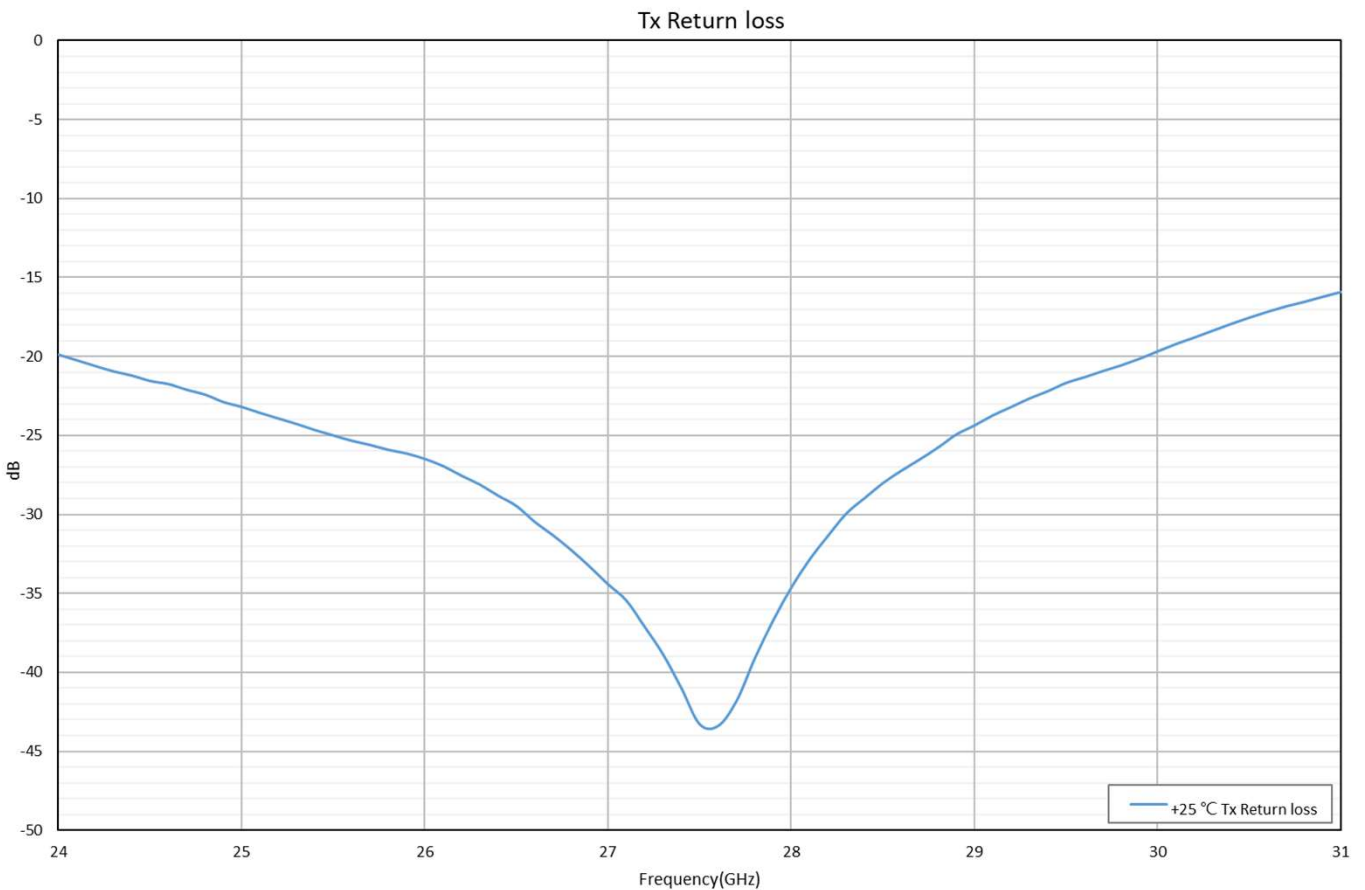
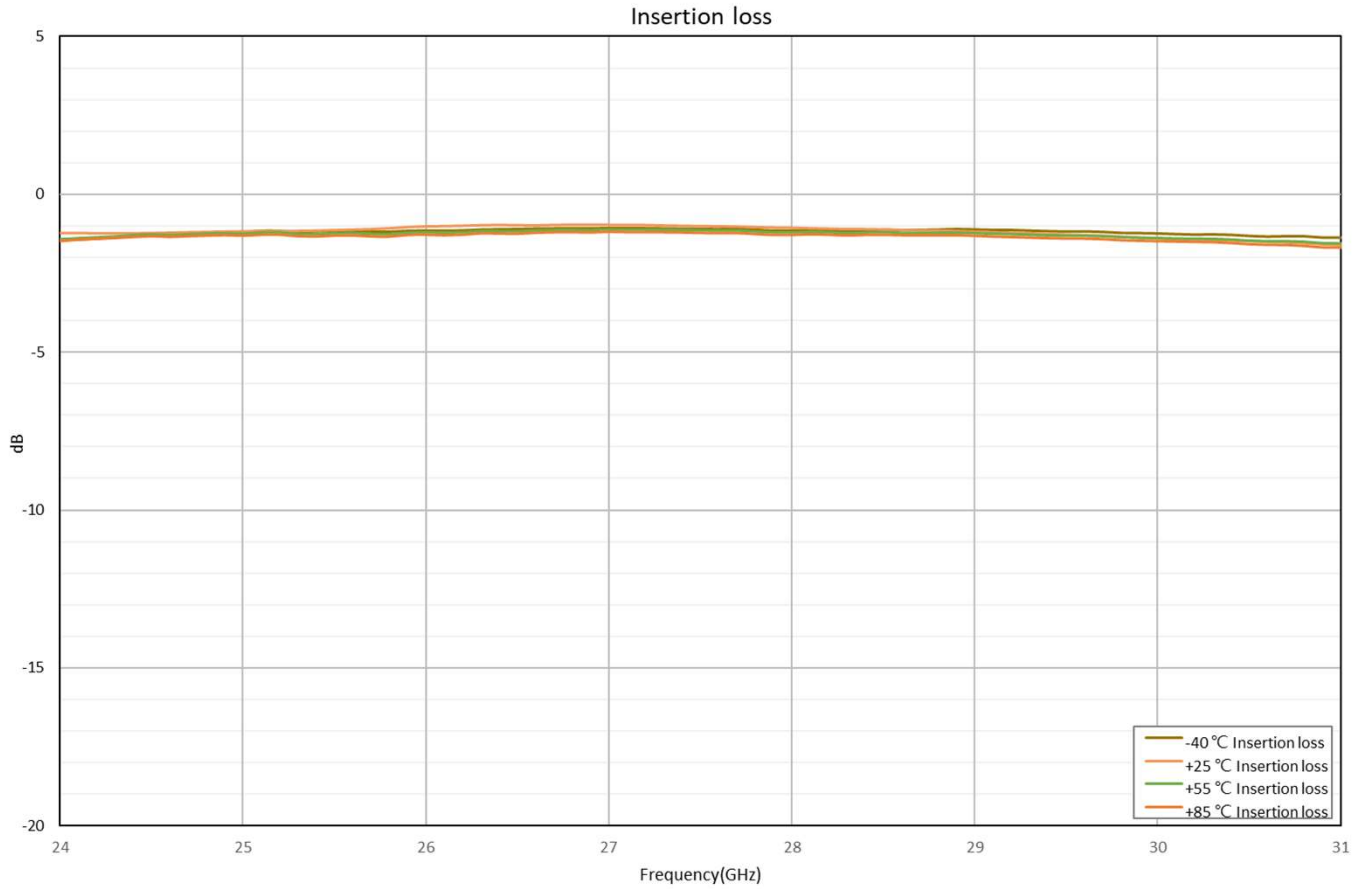


# Typical Performance Rx





# Typical Performance Tx

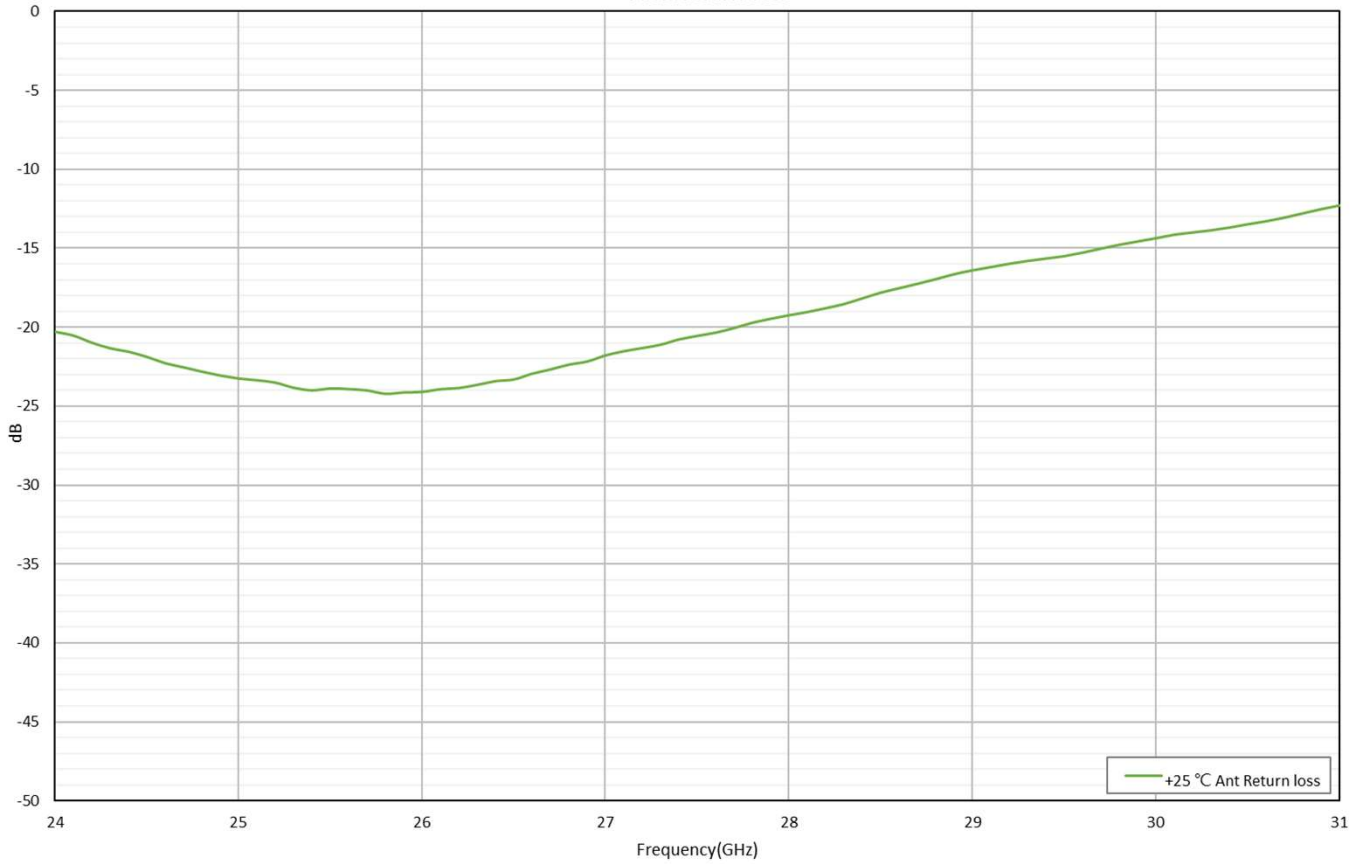




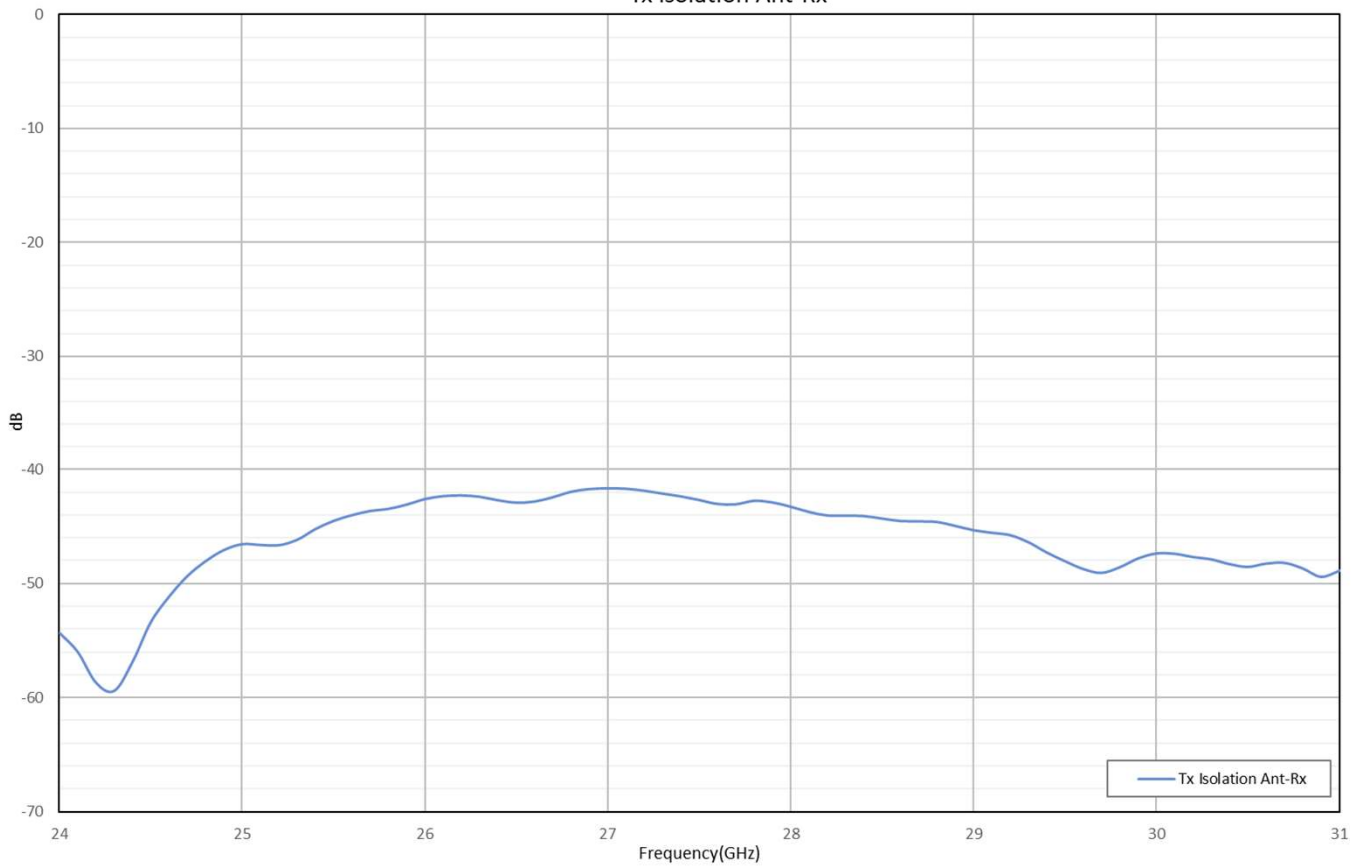


# Typical Performance Tx

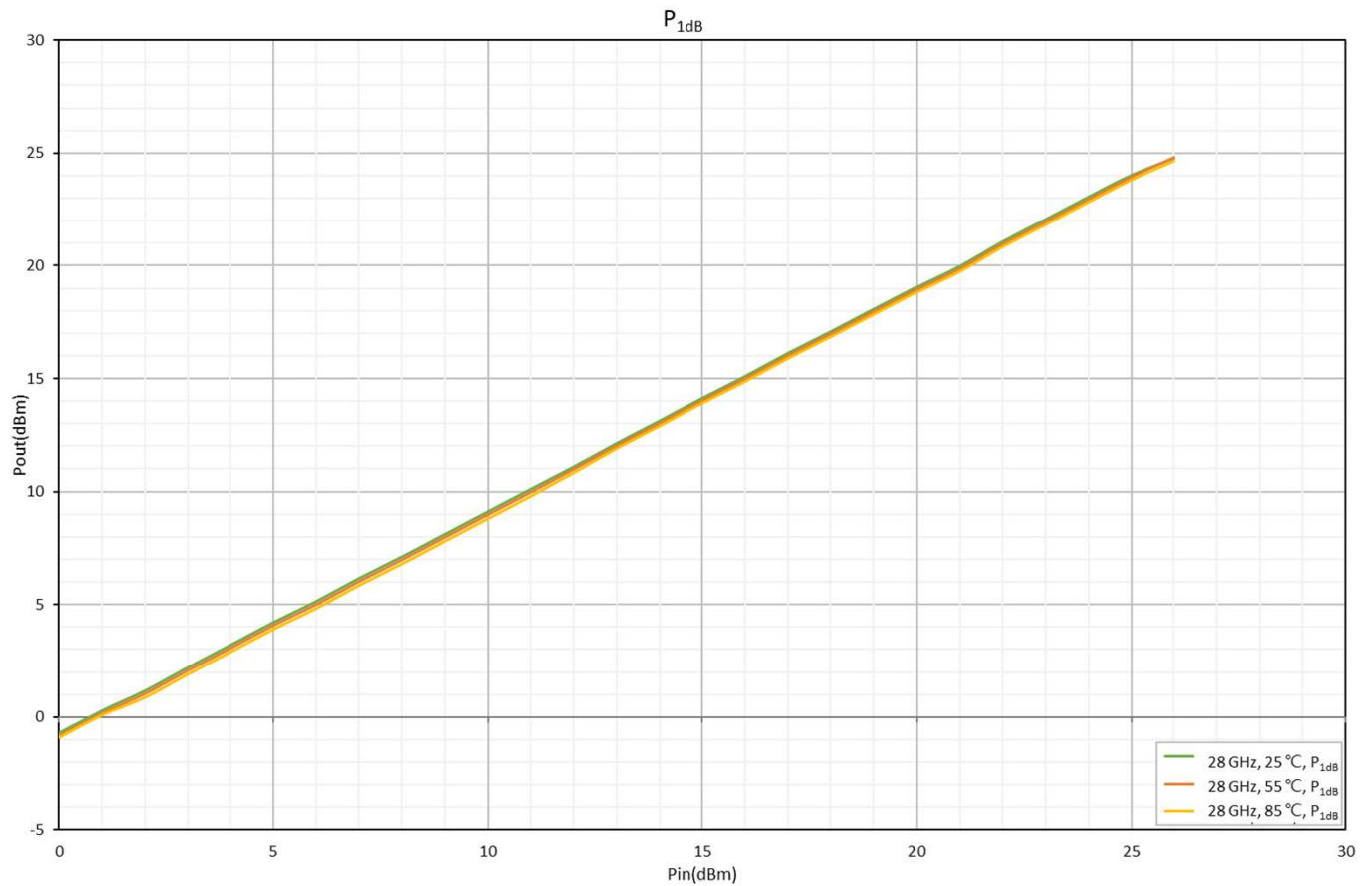
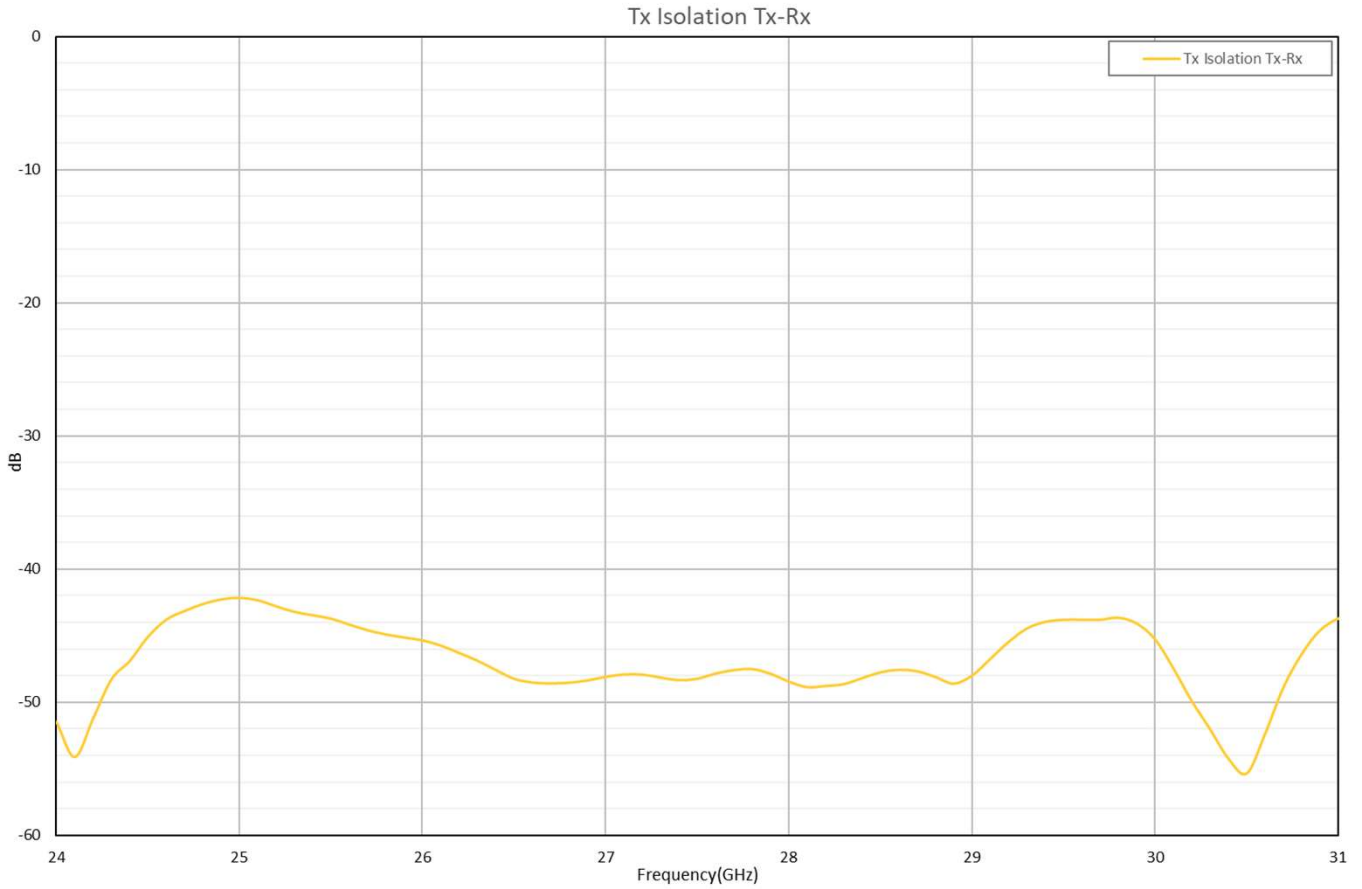
Ant Return loss



Tx Isolation Ant-Rx



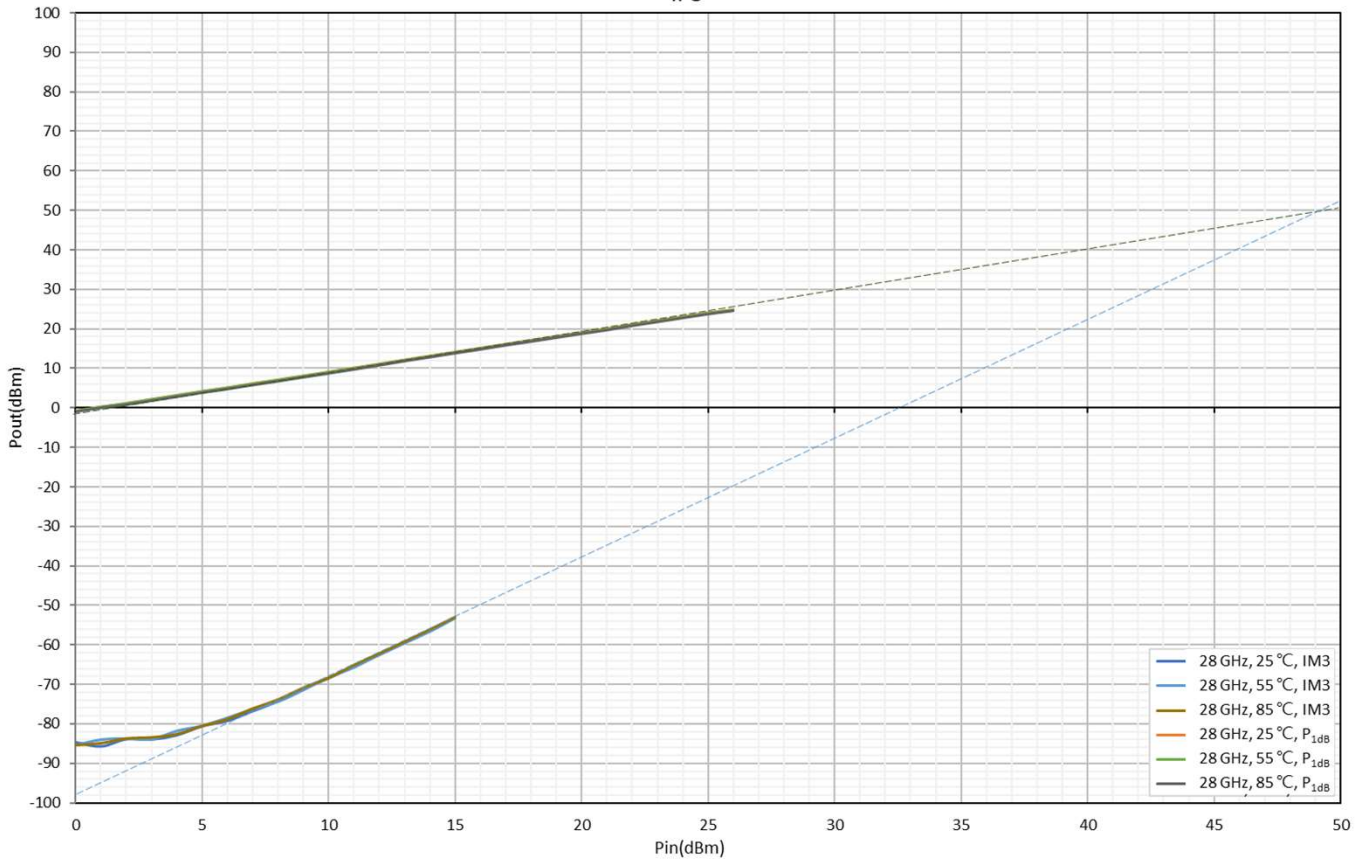
# Typical Performance Tx





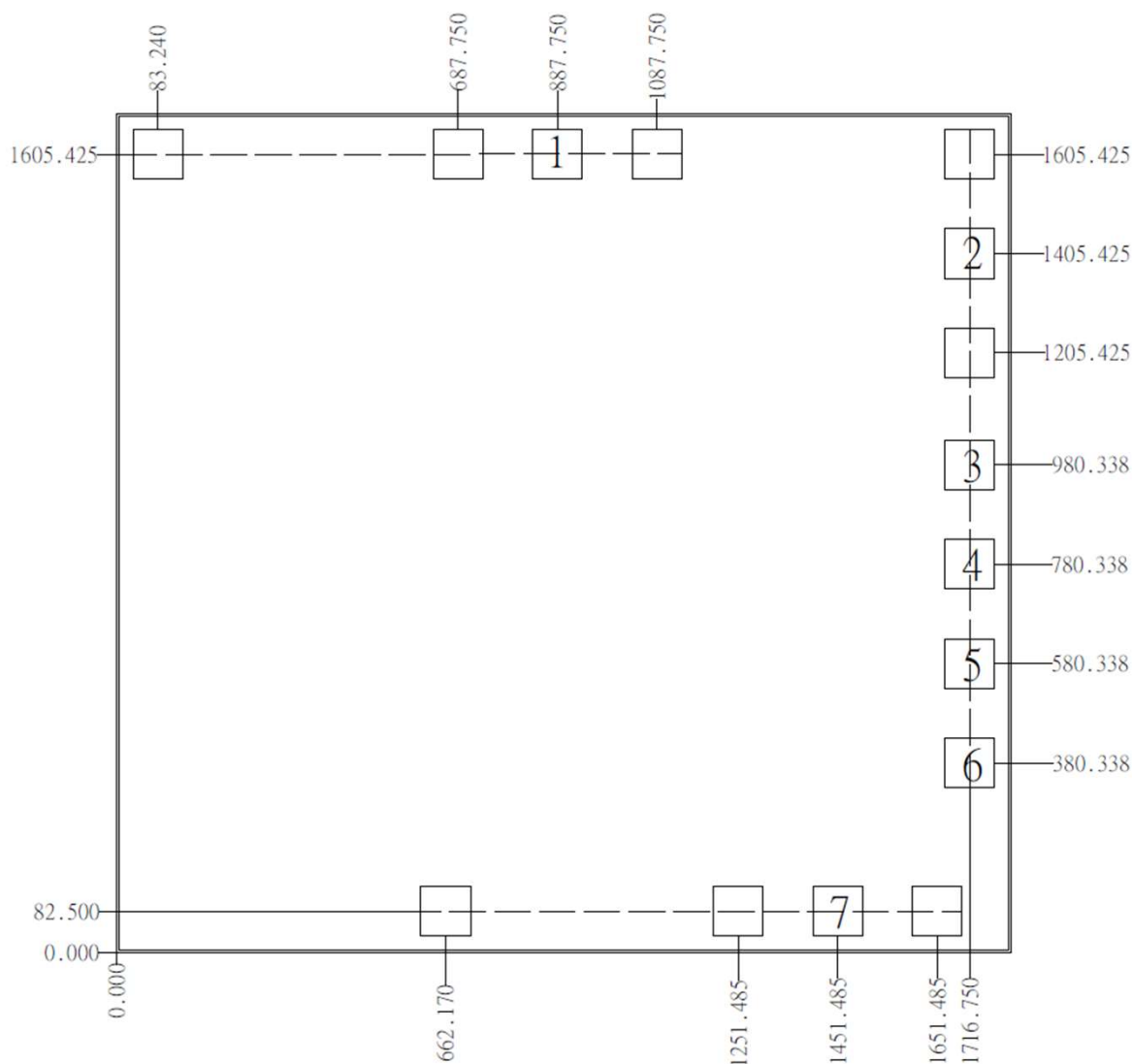
# Typical PerformanceTx

IP3





# Mechanical Information

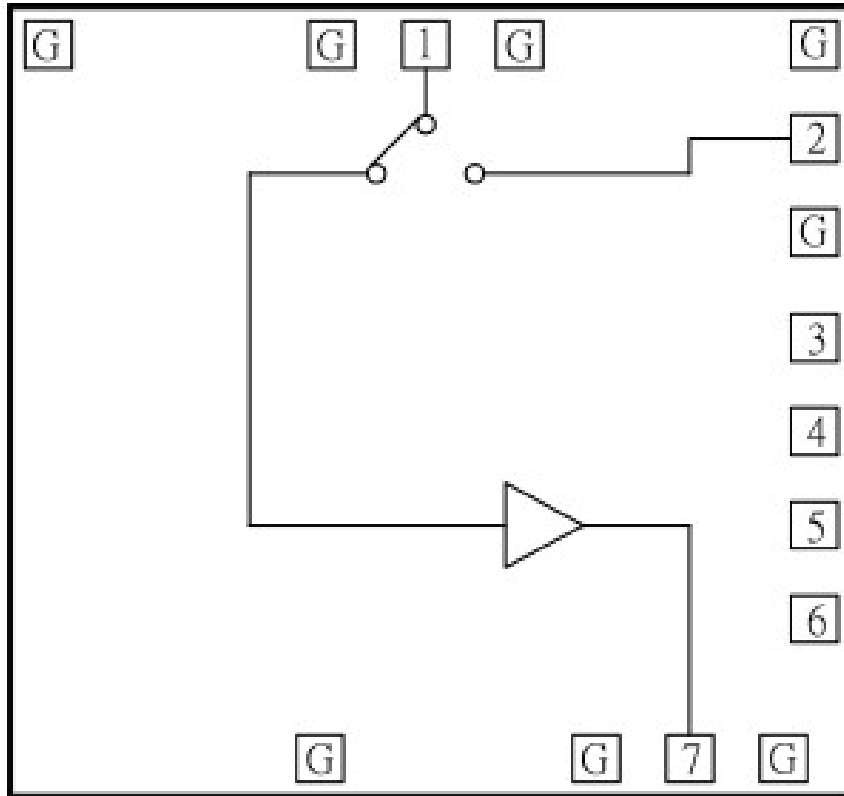


Notes:

- 1. PAD size: 100µm x 100µm
- 2. Die thickness: 100µm
- 3. Backside and bond pad metal: Gold
- 4. Backside is RF and DC ground

## Pad Description

Pad Diagram :



Pin Configuration :

PIN#	Function	Notes
1	Antenna	These pin are matched to 50Ω and Built-in DC blocks
2	Transmit input	These pin are matched to 50Ω and Built-in DC blocks
3	RxSW	See truth Table and Vbias
4	TxSW	See truth Table and Vbias
5	Drain Voltage	Drain Vbias
6	Gate Voltage	Gate Control Vbias
7	Receive output	These pin are matched to 50Ω and Built-in DC blocks
G	GND	Connect to RF and DC Ground
Backside	GND	Connect to RF and DC Ground

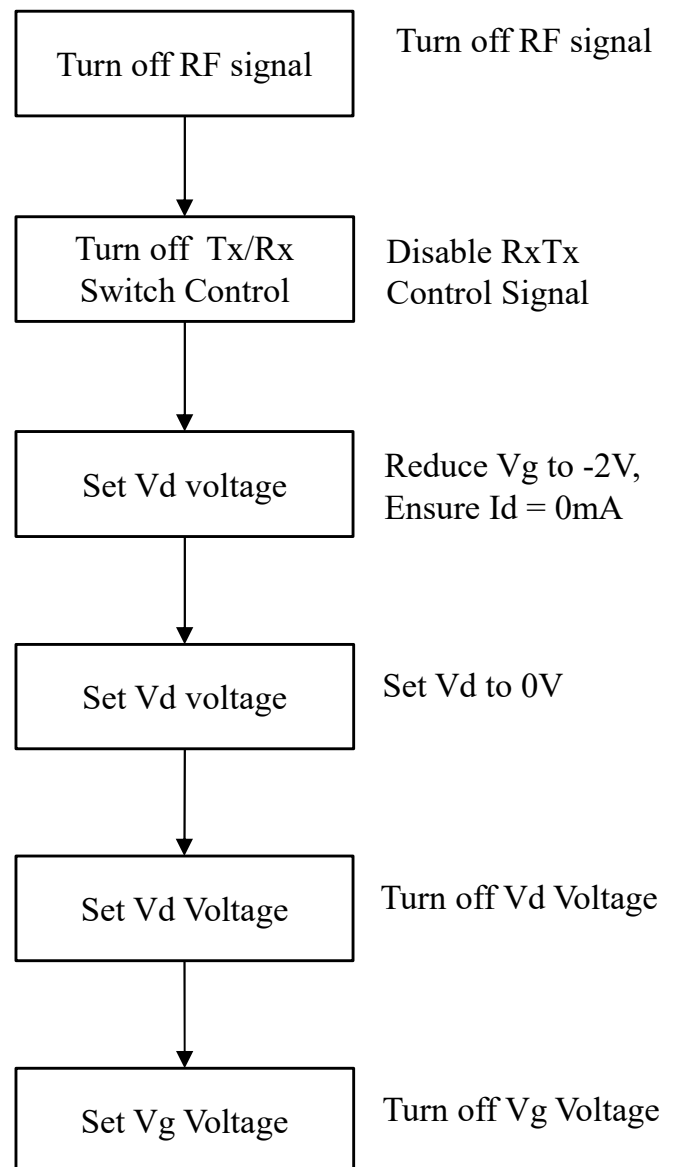
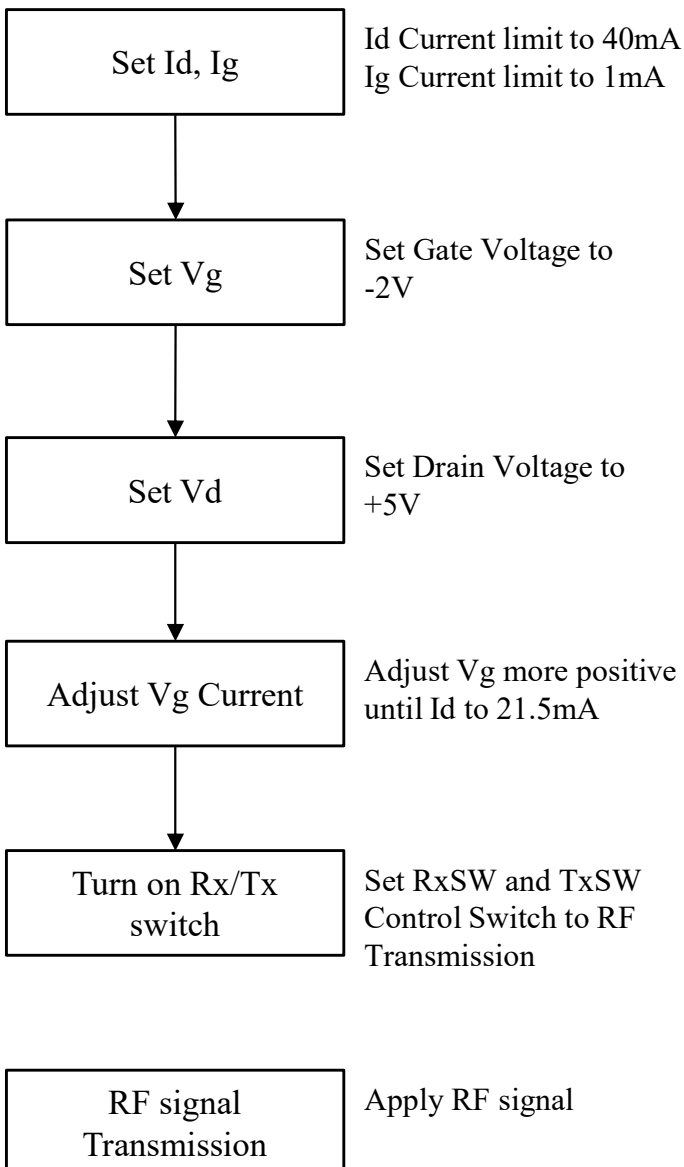
## Application Information

### LNA Bias-up Procedure:

- 1) Set Id limit to 40mA, Ig limit to 1 mA
- 2) Set Vg to -2 V
- 3) Set Vd to 5 V
- 4) Adjust Vg more positive until Id = 21.5 mA
- 5) Set RxSW and TxSW
- 6) Apply RF signal

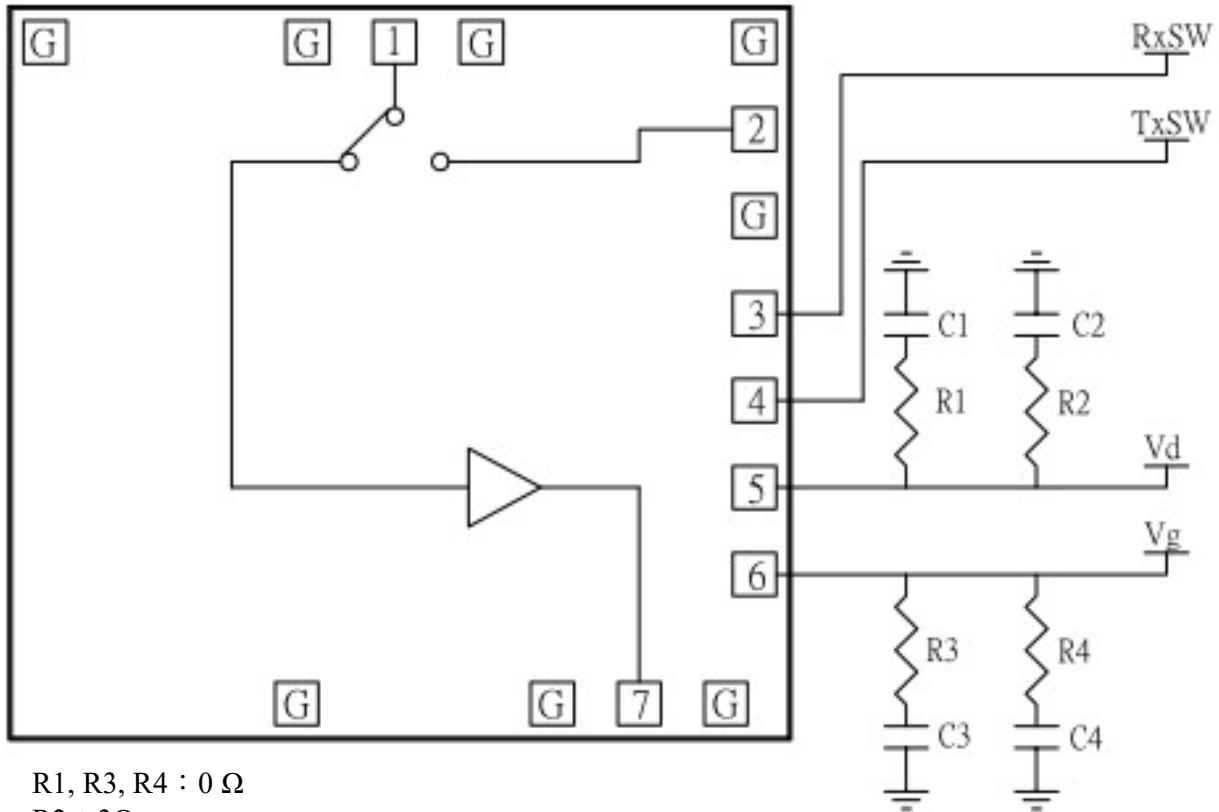
### LNA Bias-down Procedure:

- 1) Turn off RF signal
- 2) Turn off RxSW and TxSW
- 3) Reduce Vg to -2V, Ensure Id = 0mA
- 4) Set Vd to 0V
- 5) Turn off Vd supply
- 6) Turn off Vg supply



# Application Information

## Application Schematic



- R1, R3, R4 : 0 Ω
- R2 : 3Ω
- C1, C3 : 10 nF
- C2, C4 : 2.2 μF

## Application Information

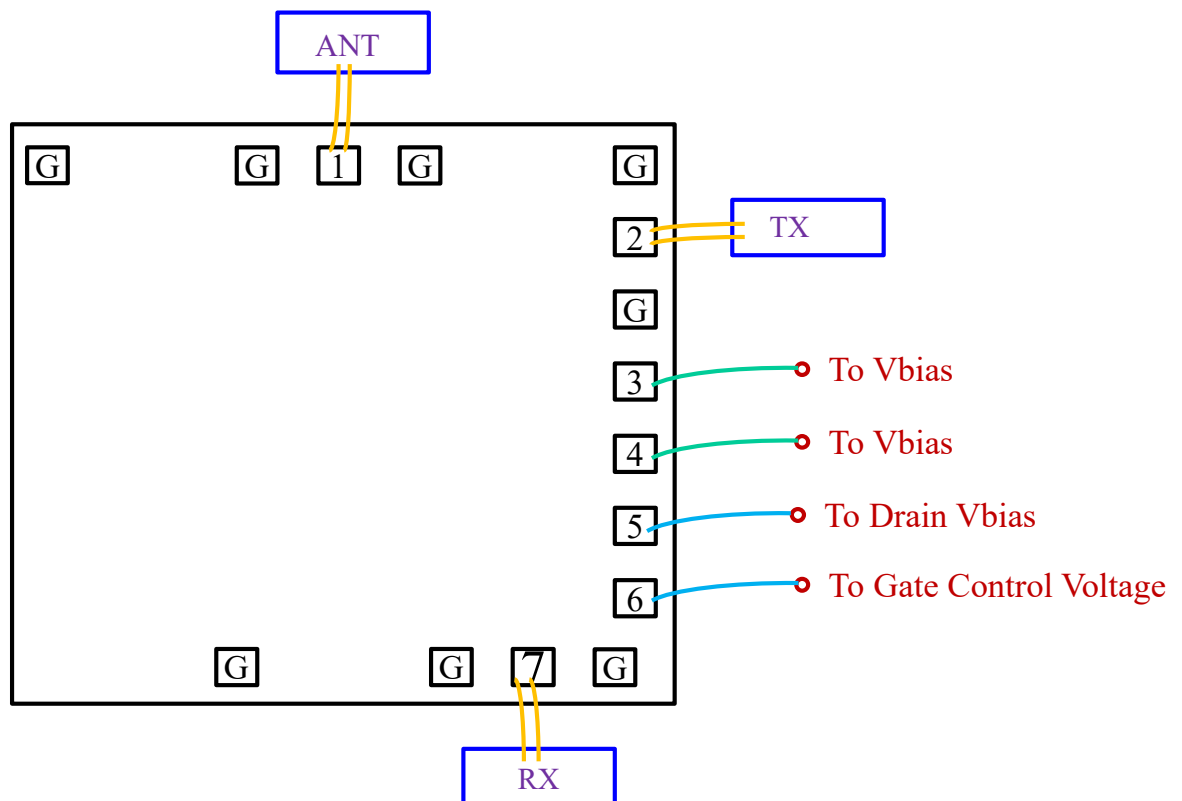
### Assembly Guidelines

The URF6C55 backside pad is RF and DC ground, die assembly operations be performed under lamellar flow or in an environment maintained at Class 1000, or better. Die attach should be accomplished with electrically and thermally conductive epoxy only, Eutectic attach is not recommended. The top surface of the semiconductor should be made planar to the adjacent RF transmission lines, and the RF decoupling capacitors placed in close proximity to the DC connections on chip.

RF connections should be made as short as possible to reduce the inductive effect of the bond wire.

The semiconductor is 100  $\mu\text{m}$  thick and should be handled by the sides of the die or with a custom collet. Do not make contact directly with the die surface as this will damage the monolithic circuitry. Handle with care.

### Assembly Diagram



Note: GaAs pHEMT dies are susceptible to chipping and cracking if not properly been handled, causing reliability concerns.





## **Static Sensitivity**

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM Class 1A devices

### **ESD Precaution:**

Protection must be afforded for the personnel, equipment, and working environment. Employees handling die must wear static dissipative wrist straps. Both the worktables and floors (or local floor mats) must be grounded to allow for static dissipation as well. Work-in-process and finished goods must be stored in an ESD protected environment. Static induced failures are often latent. The damage may not be obvious at the time of exposure of the die to ESD. Therefore, it is a good practice to insure that both the working environment and the handling techniques are compliant with the requirements for handling devices which are sensitive to ESD.

### **RoHS Compliance**

- RoHS: UltraBandTech defines “RoHS” to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, “RoHS” products are suitable for use in specified lead-free processes. UltraBandTech may reference these types of products as "Pb-Free".
- RoHS Exempt: UltraBandTech defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- Green: UltraBandTech defines “Green” to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

### **Important Notice**

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